Impact of the University Environment and VLSI Fabrication Services on Mixed-Signal Design in a University Environment

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Abstract - A university entering into the realm of mixed-signal design may encounter difficulties and the design will be impacted by several factors. Tool environments, design libraries, technology process information and VLSI fabrication service will impact the design specification and be an impediment to the successful physical implementation of a mixed-signal design and future ability to rapidly reuse the design.

Introduction

Universities that are familiar with digital design can readily create physical realizations of high level descriptions of their designs, such as VHDL, through an automated tool flow with the additional input of either a digital standard cell library for a specific technology, an FGPA environment, or sometimes the process technology information alone. Often this is enough information to rapidly generate a realization of a design for testing or verification of a digital system.

A system-on-a-chip or mixed-signal designer needs a similar path to realize their design successfully at a physical level. This is often not of interest or may even be problematic for system level designers. These projects require a community of designers to collaborate and have a common design environment and also be experienced with CAD tools and VLSI design methods. In mixed-signal this need is even more evident with the differing set of expertise between analog and digital design required for CAD tools, simulation and layout.

University Infrastructure

A quite daunting infrastructure to work with mixed-signal design needs to be created in a university environment the first time through the design process. This infrastructure includes workstations, CAD tool installation and maintenance, licenses and legal agreements, design kit installations, communication and knowledge bases, a common file convention and data structure, some form of IP sharing and archival strategy amongst colleges. User preferences and simulation and layout environments, tool training and curriculum, test and packaging strategies, test equipment, and an interface with a fabrication service are also part of the infrastructure.

The initialization and management of this infrastructure often involves many different people within the university and successful strategies are often pieced together over time depending on research needs. The designers objective is to enable a rapid transition from a high level description of a mixed-signal project to the production of a physical design and also be able to share and reuse the design easily.

CAD Tools

The topic of tools is very broad and there exists multiple valid tool flows for mixed-signal design. Typically universities support industry CAD tools like Cadence, Synopsys, Mentor Graphics, Agilent ADS, Dolphin-SMASH, Hspice, and SmartSpice. Universities are also known to support "free" CAD tools owing to the benefits of ease of the installation, support and platforms supported other than UNIX workstations. The appeal for students is the availability of this software for installation on home computers and also remote or distance learning. Tools in this category include OrCAD Pspice, MAGIC, Tanner L-Edit, Alliance, ELECTRIC, and MyCAD and PC based layout tools like LASI and Microwind. These tools typically suffer from not being able to handle larger industrial strength designs or the detail work like extraction and verification or even providing a path to generating a layout.

The learning curve for industrial design automation tools is manageable by most students in a university environment when accompanied with some introductory training and tied to assignments and projects in design courses. Students benefit from gaining experience with industrial design tools that can be applied to work experiences during their research. The opportunity for students to bring back best practices from their work assignments and establish these as local practices is also a strong advantage.

Industry benefits from better training of students in circuit design and layout. The final compelling reason to adopt industry compatible tool flows is the problem that often arises when university research tries to interface with external projects and tool compatibly issues may result in lengthy delays.

The Cadence framework is popular because of its ability to interface with external tools, such as program written by researchers. Cadence provides one environment where the layout information can be organized along with the different types of models of digital or analog circuits. Integration of the Analog Artist simulation within the Cadence design environment is an advantage for mixed-signal simulations where accurate analog simulations are needed as well as mixed mode and/or behavioral simulations. Verification, library management, and back annotation also occur within the same framework.

Design Kits

Rapid scaling of new generations of technologies forces the microelectronic communities in mixed-signal to need access to up-to-date processes. Besides working with cutting edge CMOS technologies, mixed-signal designs are often candidates for "niche processes," SiGe, GaAs, or SOI processes which are needed to meet the analog requirements.

Design kits available for university use are sometimes lacking and often the availability is determined by cost or industrial partnerships. Many different digital libraries exist and are sometime provided by the foundry for which the design is targeting. In the university environment, often there is not a choice of libraries and users are forced to make do with whatever is available.

For mixed-signal design, there are additional concerns with respect to a design kit. Beyond parameterized device cells and digital layouts, a mixed-signal kit needs to support additional considerations, such as:

- Accurate device models and corner models for Monte Carlo simulations
- Analog passives such as inductors, accurate capacitors, high valued resistors, varactors and diodes
- Ability to simulate multiple supply domains and analog ground
- Specialized I/Os that support analog performance requirements
- Padframes that support multiple supply rail voltages and/or large analog macros
- Isolation structures and more accurate extraction for cross-coupling
- Automated wire routing between analog and digital blocks
- Behavioral simulation environment support
- Verification support for full chip DRC and LVS

VLSI Fabrication Services

The most familiar VLSI fabrication service is MOSIS which supports US universities. The fabrication service serves as the middleman to the actual foundries and provides a low-cost environment for multi-project fabrication in leading edge process technologies. The cost of NRE, masks, wafers, packaging and test is shared by combing multiple projects. VLSI fabrication services take care of merging designs, placing orders, mask data preparation, product tracking and delivery. Often classes and tool training are part of the services.

MOSIS handles the Multi-Project Wafer setup and provides a central focal point for technology information, design libraries, models, digital layouts, I/Os and padframe layouts in the fabrication technologies they support. Most university designs fabricated through MOSIS are typically very small area and have a limited pin count.

Outside the US, there are several VLSI Fabrication Services available to universities (See Table 1). These fabrication services vary in the level of support offered, but they all provide their members with access to similar industry processes. The fabrication services support a similar set of the major industry CAD tools as MOSIS.

Other VLSI fabrication services may incorporate the design kits and tools into their services, providing a single interface to EDA vendors. Many fabrication services take care of rental of CAD software through their budgets and provide them nearly free of charge to university and then require registration and small maintenance fees. Some services, like Canadian Microelectronics Corp. (CMC) and EUROPRACTICE maintain computing labs and support for workstations and CAD tools. Some of the organizations also provide hardware and test facilities. Different levels of training and workshops are provided by the different service organizations along with the development of textbooks and materials for VLSI and system design to be shared with other university.

An opportunity exists for these organizations to have even greater value add by moving further up the design flow and provide more robust design environments which are uniform and compatible, thereby enabling a university to collaborate with other universities and industry projects. Such organizations could serve as a central IP center for university collaborations and provide guidelines of common ways of defining mixed-signal designs for understandability and storing data for reuse.

Documentation

Currently, there are limitations on industry tools to create publication worthy documentation and a reusable description of designs. In order to enable rapid reuse, mixed-signal designs need to be able to document all the consideration that went into the design, such as cross-talk, matching considerations in layouts, bias voltage calculations, etc. Test documentation is of concern because quite often, different students perform the testing at a later date then the designers of the project.

Conclusion

University programs desiring to tackle such designs as Unmanned Airborne Vehicles or wireless sensor networks need to enable an environment which supports the digital and analog simulation as well as being aware of the impact the process technology, CAD tools, and design kits will have on the system design. Mixed-signal designers must be able to maneuver through such obstacles to efficiently meet the original mixed-signal specifications. As shown in Figure 1, there must be consideration given to these impediments.

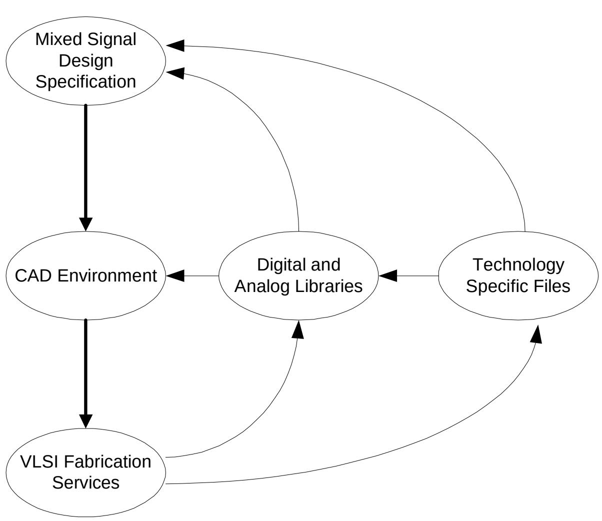

FIGURE 1: Downstream Impact on Specification

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Table 1: VLSI Fabrication Services Comparison

VLSI Fabrication Service	**Foundry Technology Supported**	**CAD Layout Tools Supported**
MOSIS *[USA]*	Agilent 0.5u AMI 0.5u, 1.5u AMS 0.8u SiGe IBM 0.5u SiGe Peregrine 0.5u SOI PML GaAs HEMT 0.2u TSMC 0.35u, 0.25u, 0.18u	Cadence, Mentor Graphics, Tanner/L-Edit, Ballistic, Electric, LASI, Magic, IC Editor
CMP (Circuits Multi-Projects) *[France]*	AMS 0.8u, 0.6u, 0.35u AMS 0.8u SiGe, BiCMOS Peregrine 0.5u SOI PML GaAs HEMT 0.2u STM 0.25u, 0.18u	Alliance, Cadence, Mentor Graphics, Synopsys, Tanner/L-Edit, Eldo,
CMC (Canadian Microelectronics Corp.)	TSMC 0.35u, 0.25u, 0.18u Mitel 1.5u	Synopsys, Cadence
EUROPRACTICE *[Europe]*	Alcatel 2.0u, 0.7u, 0.5u, Alcatel 2.0u, 1.2u HBIMOS AMS 0.8u, 0.6u, 0.35u AMS 0.8u SiGe ESM 0.5u UMC 0.25u, 0.18u, 0.13u	Altera, Cadence, Mentor Graphics, Synopsys, Tanner/L-Edit
IDEC (IC Design Education Center) *[Korea]*	LG Semi 0.6u Hyundai 0.65 Anam Semi 0.25u	Synopsys, Mentor Graphics, Silicon Ensemble
VDEC (VLSI Design & Education Center) *[Japan]*	HHS 0.5u Hitachi 0.35u Motorola 1.2u NEL 0.5u Rohm 0.6u, 0.35u	Synopsys, Cadence, Mentor Graphics
CIC (Chip Implementation Center) *[Taiwan]*	Alcatel 2.0 HV AMS 0.8u PML GaAs HEMT 0.2u	Cadence, Synopsys