



*Department of Electrical and Computer Engineering
Colloquium*

**Static Analysis of High Level System Descriptions for
Taming Verification Complexity**

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The growing complexity of VLSI and System-on-a-chip(SoC) designs has made their verification extremely expensive, time-consuming and resource intensive. Formal verification of system behavior is critical to the design cycle due to its ability to isolate subtle flaws and provide high quality assurance. However, its computational intractability limits applicability in practice, rendering the state-of-the-art grossly insufficient to meet the needs of the industry. In this talk, I will present a suite of techniques that are a significant departure from traditional Boolean level approaches to formal verification. The algorithms are based on a top-down, domain-specific perspective of the system by reasoning at the system level and register transfer level descriptions. Static analysis of these high level system descriptions using structural information and symbolic reasoning leads to effective decomposition strategies that create tractable portions of the system. These manageable system components can then be verified by deploying efficient Boolean level algorithms.

Since the static analysis techniques exploit the expressiveness and design information available at the higher level, each technique has a corresponding application domain. I will discuss antecedent conditioned slicing and its application to property checking in the context of pipelined processor verification. I will also discuss comparison point theory using term rewriting systems, its application to equivalence checking, and demonstrate the benefits in the context of multiplier and SoC verification.

Biography: Shobha Vasudevan is currently doing her Ph.D at The University of Texas at Austin. She received an M.S.E. degree in Computer Engineering in 2003 from The University of Texas at Austin, and a B.E. degree from the University of Mumbai, India. Her research interests are in formal and semi-formal verification of VLSI and embedded systems, VLSI and SoC testing, system level power management and software verification.