

ECE323 Final Design Report Guidelines.

1. Perform a design report comparing a MOS inverting amplifier in Figure 1 to one where a BJT substitutes for the MOSFET. Compare and contrast gain, bandwidth, and settling time. For the MOS case, this is known as a common source amplifier, while for the BJT, this is a common emitter amplifier.
2. Compare the common source behavior to the MOS differential pair amplifier circuit in Figure 2, as shown on the last page. Compare DC, AC, and transient behavior.
3. Add negative feedback to both the common source and differential pair amplifiers to create inverting amplifiers. Compare AC behavior with and without feedback.

The report should have the following sections:

Abstract – write this last, it's the main things the reader wants to know.
Short problem statement and its answers.

Introduction – Problem context, requirements, and set up.

Results and Discussion – All the technical details.

Conclusion – Review your main results.

The main section is Results and Discussion. This section contains your detailed technical content, such as simulation set ups, plots, tables, hand calculations, and your explanations of your technical content. For example, every plot or figure should have some sentences which direct the reader to the main point of the plot or figure.

Hints for the design work.

Do a DC transfer curve at several V_b values to find useful bias points for V_{in} .

Run an AC analysis at the bias point you found.

Run a transient analysis to compare to your AC analysis.

Hand Calculations are similar to what you were asked to do for common source amplifiers. The differential pair behaves very much like a common source amplifier. This is discussed in section 7.2 if you want more detail.

From a more simple approach, the 3dB frequency is the same result we've seen in a low pass filter, equal to $1/RC$.

For the AC gain at low frequencies, the gain is equal to $gm \cdot R/2$, as shown in equ. 7.32

The $1/2$ factor is because V_{in} is divided evenly in half by the two matched transistors in the differential pair. This is explained in ece720.

To find gm for MOS you use the same formulas as before, $gm = 2 \cdot I_b / V_{ov}$. For a BJT, use $gm = I_b / 25mV$ (thermal voltage).

I_b is the bias current, and $V_{ov} = V_{GS} - V_t$, where V_{GS} is the dc value. (V_{ov} is the voltage over V_t , same as $V_{effective}$).

As long as the DC voltage to both input transistors are the same, each transistor will have $1/2$ of the total bias current, eg. $40\mu A = 0.5 \cdot 80\mu A$. This is the main advantage of this circuit, the DC input voltage can be adjusted and the bias is independent of V_t .

To find V_{ov} , set $I_b = (1/2) \cdot k_p \cdot (W/L) \cdot (V_{ov})^2$ and solve for V_{ov} . Note that W/L is 100, and you can set k_p in the nmos model (the TopSpice default is $k_p = 20\mu A/V^2$).

Finally, keep in mind this circuit is just the main part of an op amp. A better op amp is shown in figure 9.1, where the input transistors are pMOS instead of nMOS. pMOS inputs are often used, that's why we studied the pMOS common source amp. Figure 9.1 shows a second amplifier stage after the diff. Pair. The second stage can have a gain of about 20, so it's input doesn't need to vary by more than 0.25v (for 5v supply). That means the differential pair output doesn't need to vary by more than 0.25v, so it's not a problem that the outputs you see in the DC sweep have a limited useful range of 1-2volts at different V_b settings. It's more than enough.

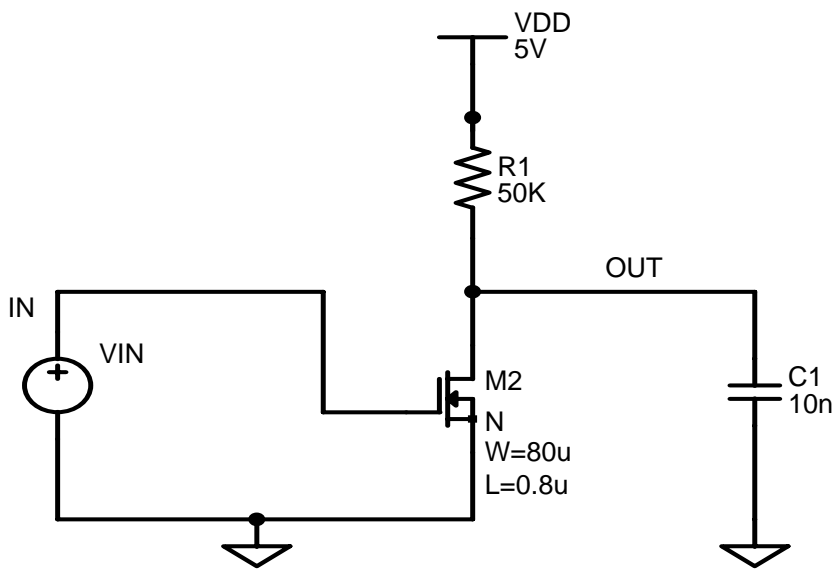


Fig. 1. Common source inverting amplifier.

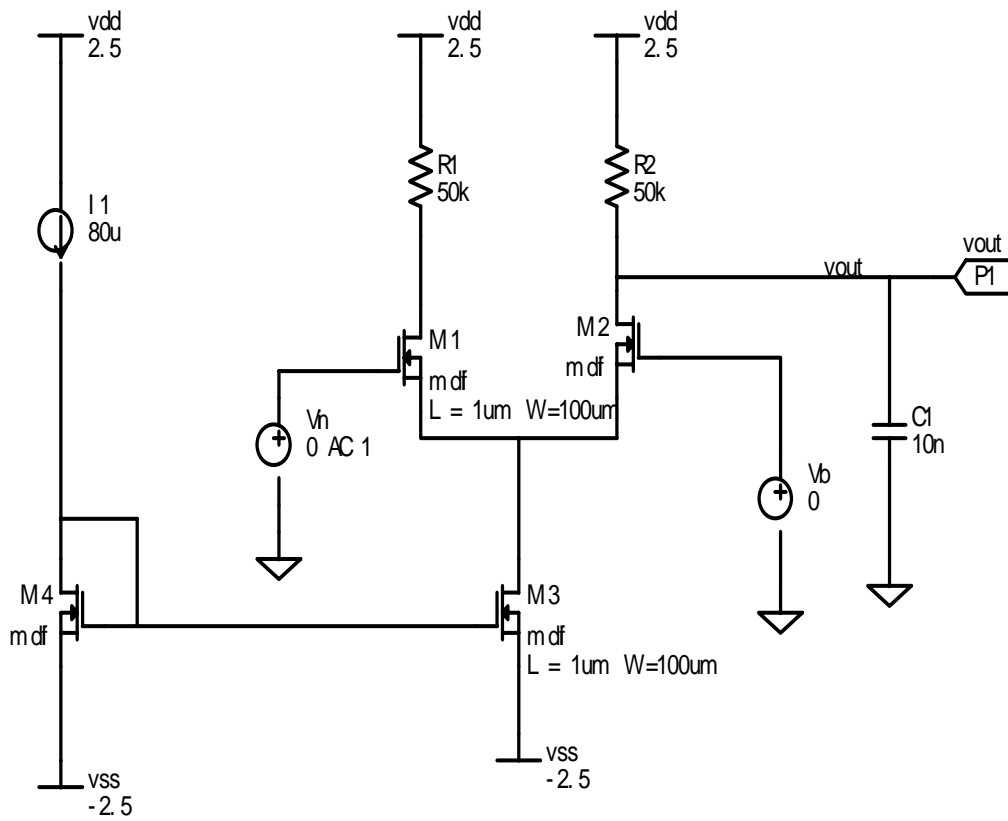


Figure 2. Differential pair amplifier