

ECE 582: Electrical and Computer Engineering Design I

Lecture 1: Digital Library Project Overview

Prof. Steven Bibyk (683)

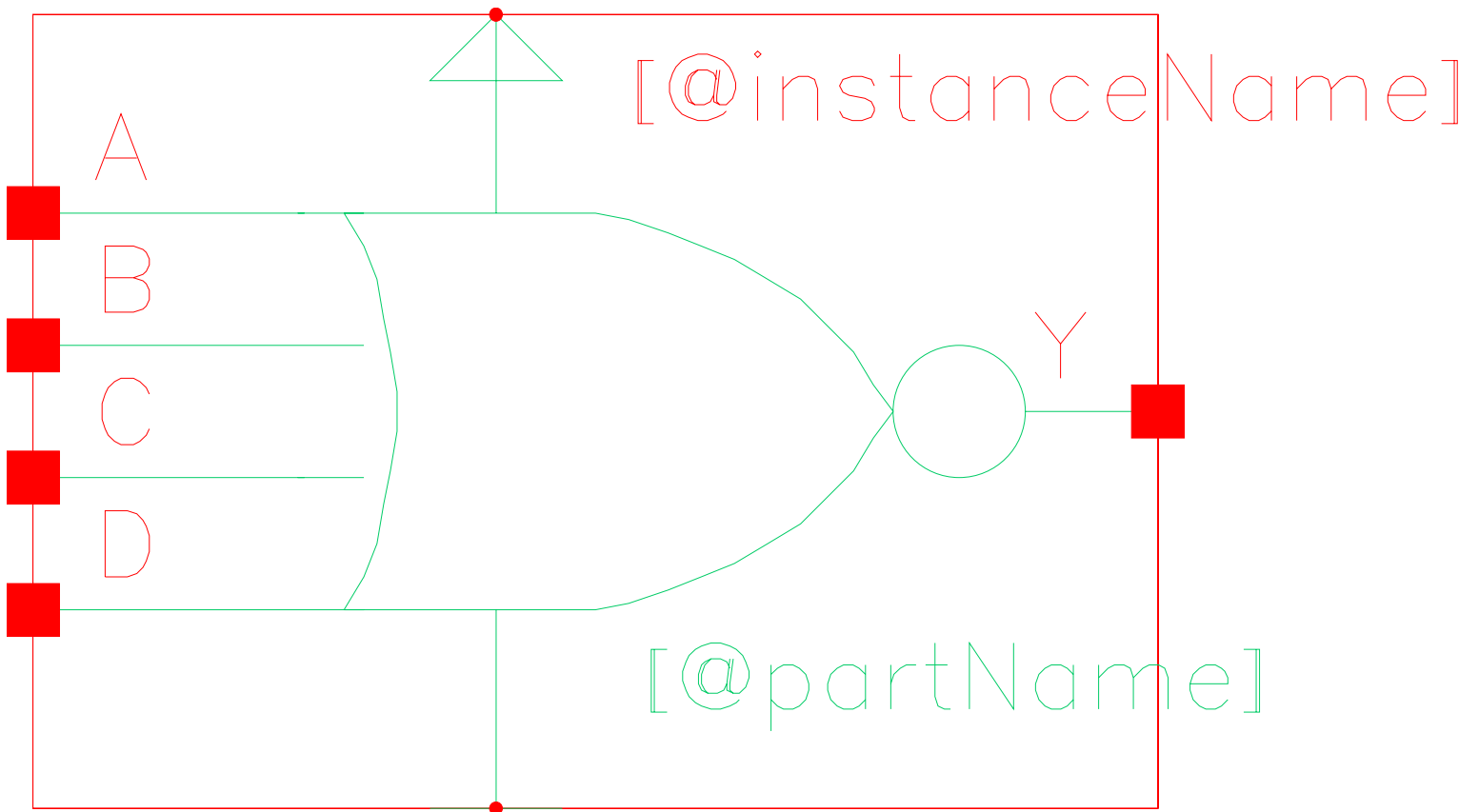
TA: Brian Dupaix

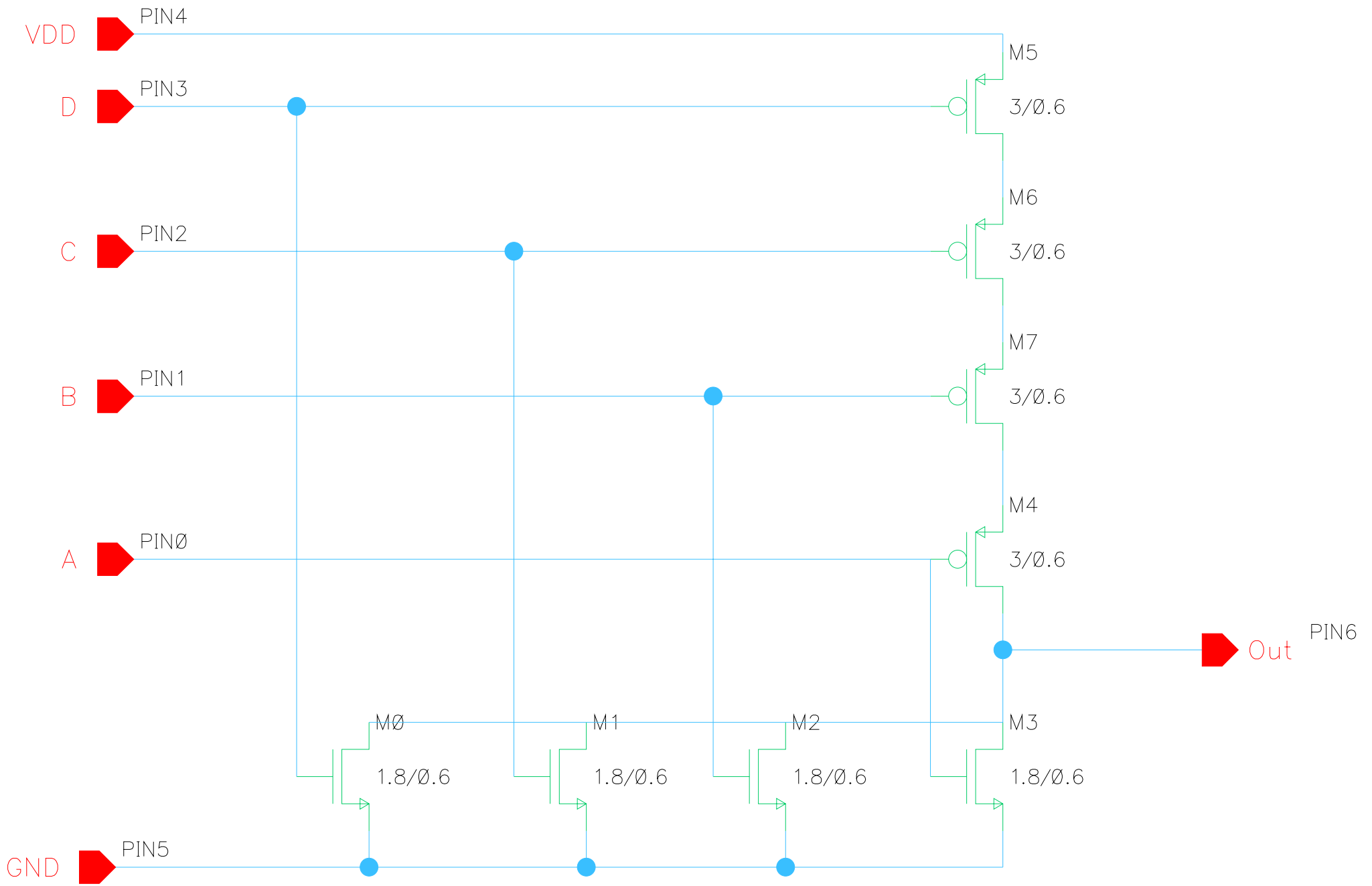
September 27th, 2005



Project Overview I

- Required to take ECE 720 (Wi) or ECE 721 (Sp)
- Develop cells to add to the OSU digital library
 - 582 work
 - Learn Cadence toolset.
 - Schematic Capture
 - Transistor simulation
 - Basic Layout
 - Learn how to design digital cells using transistors
 - Learn basic concepts of timing, fanout, capacitive loading
 - Learn how transistors are formed on silicon wafers
 - Create transistor level schematic in cadence.





Project Overview II

- 683 work
 - Simulate and validate transistor level schematic design
 - Design and Capture cell Layout
 - Generate Timing information for cell
 - Create HDL model for cell (Verilog/VHDL)
 - Prepare cell for fabrication
- A test chip containing all current cells will be sent to MOSIS for fabrication at the end of Spring Quarter.

