

# **ECE 683 Analog Group Report**

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## Table of Contents

<b>Executive summary</b> .....	3
<b>Introduction</b> .....	4
<b>Differential Amplifiers</b> .....	5
<b>Figure 1 Symbol for a single-ended-output Differential Amplifier</b> .....	5
<b>Analog to Digital Converter</b> .....	9
<b>Figure 2 Functional Block Diagram (16Bit)</b> .....	10
<b>Figure 3 Functional Block Diagram (12Bit)</b> .....	11
<b>Digital to Analog Converter</b> .....	12
<b>Figure 4 Symbol of CDAC10_C35 Digital to Analog Converter</b> .....	15
<b>Figure 5 HS mode at fclk = 100MHz</b> .....	16
<b>Figure 6 LS mode at fclk = 100MHz</b> .....	16
<b>Standard Cell Library</b> .....	16
<b>Table 1 List of Cells Distributed (Virginia Tech.)</b> .....	20
<b>Design Work</b> .....	21
<b>Figure 7 A sample differential amplifier schematic</b> .....	21
<b>Figure 8 The differential amplifier symbol</b> .....	22
<b>Figure 9 A circuit using the new differential amplifier symbol</b> .....	23
<b>Licensing Agreement</b> .....	23
<b>Conclusion</b> .....	26

## **Executive Summary**

For the ECE 683 VLSI design project, the group has a variety of tasks related to the process of specifying and licensing Intellectual Property in the form of analog and digital circuits.

Much of the work consists of descriptions and breakdowns of various logical structures. The first structure being discussed is an Analog-to-Digital converter, or ADC. Group members describe the functionality of the ADC, and include various examples and schematics to show how it works. Next, the Digital-to-Analog converter, or DAC, is examined in detail. Like the ADC, it is accompanied by several schematics and samples to help better show the functionality. The final structure is the amplifier. Several different amplifiers are included, such as fully versus partially differentiated amplifiers. Different design approaches are also included, such as those optimized for speed as opposed to power.

The next tasks in the project are quite different from the first ones. The first of these tasks involves repeated correspondence between various fabrication companies such as AMI, IBM, and MOSIS. Many of these companies have been reluctant to release information regarding analog cell development, but the replies from the cooperative companies help to paint a good picture of the lack of development in the Analog Cell Library field. The next task is to explain the restrictions and guarantees explicitly stated in the non-disclosure and confidentiality agreements required by the companies to license their software. These documents provide a wealth of information regarding the rights and responsibilities of both licensees and licensors. The final task is the creation of a symbol

using cadence design software. In the group's design, a differential amplifier was used to create the symbol.

The report of this project begins with a table of contents. It then gives an introduction to the main topics of the report, including a description of the problem, as well as the purpose and scope of the project. Next, the Background Research section contains the main descriptions of the work involved for each group member, as described in the paragraphs above. Following the Background Research section, the Design section shows the actual created material of the project, which in this case is a symbol for a differential amplifier. Finally, the conclusion summarizes the main ideas contained in the report, and brings it all together.

## **Introduction**

This paper intends to discuss the organization of three existing analog cell libraries. The cell libraries studied include those created by Virginia Tech and Oklahoma State University, as well as those developed by Tanner CES (available from Analog Devices inc and National Semiconductor). Precise device specifications and schematics were impossible to come by (due to the difficult and secretive nature of analog VLSI cell design), and so published specifications of the libraries available online were used instead. At the top level, each of the analog cell libraries divided themselves into three distinguishable component types: differential amplifiers, analog to digital converters (ADCs), and digital to analog converters (DACs). This paper will discuss the organization of differential amplifiers, ADCs, DACs. Also in this paper, we will mention about licensing agreement of analog cell library.

This paper includes example of differential amplifier by Cadence and its symbol.

## Differential Amplifiers

Differential Amplifiers refer to an analog circuit component that can be used to amplify a signal or be used as an op-amp to apply a transformation onto a voltage signal. A differential amplifier amplifies the voltage difference between two input terminals, usually referred to as positive (+) and negative (-). Differential Amplifiers come in two varieties: single-ended-output amplifiers, whose one output pin gives the voltage difference in respect to ground, and fully-differential amplifiers, whose two output pins give the voltage difference in respect to each other. The symbol for a differential amplifier is shown below as Figure 1.



**Figure 1: Symbol for a single-ended-output Differential Amplifier**

### Single-Ended-Output Amplifiers vs Fully Differential Amplifiers

In discrete analog design, single-ended amplifiers are more often used since they are easier to design with. In VLSI analog design, however, fully-differential amplifiers are more often used than single-ended as they provide several significant advantages, such as immunity to external noise and increased output performance.

Fully-differential amplifiers have an immunity noise because of common mode rejection. Common Mode Rejection is the ability of a balanced (or differential) input to reject the part of the incoming signal which has the same amplitude and phase on both input terminals. In other words, it is the ability to respond to only differences at the input terminals.

In addition to the ability to reject noise, differential amplifiers are also capable of increased performance due to higher output gain, a larger signal swing, and reduced second-order harmonics. All three of these improvements are due to the elimination of the mirror pole found in the gain stage of the single-ended-output amplifier. The elimination of the mirror pole allows both output stages to be used, increasing the dynamic gain by 6dB. In addition, the elimination of a pole in the gain block's transfer function reduces second order harmonics which in turn increases the gain bandwidth of the amplifier.

### **Parameters of a Differential Amplifier Design**

Besides choosing whether to use a single-ended-output amplifier or a fully-differential amplifier, an analog VLSI designer must also decide which other amplifier characteristics

are important for their design. These characteristics can be separated and classified as design parameters, such as voltage gain, slew rate, supply voltage, offset voltage, signal swing, and power dissipation. While a given amplifier design might be optimized for just a few parameters, any given analog cell library will have hundreds of different parameter combinations available to choose from. In order to understand how these parameter combinations relate to each other, it is important to understand what each of the most important parameters mean:

### **Voltage Gain**

Gain is the ratio of the differential amplifier's output voltage compared to input voltage, and is usually expressed in decibels. An amplifier's voltage gain may be as high as 80dB or as low as 10dB depending on the design.

### **Slew Rate / Speed**

Slew rate is the maximum rate at which a differential amplifier's output can change, and it is generally expressed in V/ $\mu$ s. Slew rate can also be thought of as the slope in an amplifier's output when given a square-wave input. As such, slew rate defines the speed of a differential amplifier. Although it would be ideal for the slew rate of an amplifier's to be identical from high-to-low (HL) and low-to-high (LH), this is often not the case, and so the slew rate for both is often given. The slew rate will be around 0.5V/ $\mu$ s for a slow amplifier, and as high as 30V/ $\mu$ s for a fast amplifier.

### **Supply Voltage Range**

Supply voltage refers to the allowable range of values used for  $V_{dd}$  and  $V_{ss}$ . In some amplifiers, this range is as large as +15V to -15V, while in others (such as low-power designs) it may be as low as +1.5V to -1.5V. Supply voltage is also directly related to the average power dissipation of an amplifier.

### **Offset Voltage**

An amplifier's offset voltage is an amount of DC voltage that is added to the output signal. For most amplifiers, this DC offset voltage is ideally zero, but is implemented to be in the range of 0.5-10mV. Some amplifiers, however, are designed to have a very large DC offset voltage, in the range of  $(V_{dd}-V_{ss})/2$ .

### **Signal Swing**

The signal swing for a differential amplifier is range for which an input signal can be amplified without becoming saturated to the supply voltage. The ideal signal swing for any amplifier would be from  $V_{ss}$  up to  $V_{dd}$ , but that is impossible to implement in any real amplifier. Signal swing is most important when dealing with devices that have very small (under 3V) power supplies.

### **Power Dissipation**

Power dissipation refers to how much power is consumed by the amplifier per second given an input signal in the average range of operation.

### **Gain Bandwidth**

Gain bandwidth refers to the range for which the amplifier's voltage gain can be considered a reasonable estimate. The internal transfer function of a differential amplifier causes it to act like a low-pass filter, and so the 3-dB frequency of this filter defines the gain bandwidth of the amplifier.

### **Special Function Types**

In addition to classification by design parameters, some differential amplifiers are classified to have a specific purpose. For instance, all of the cell libraries that were studied contained analog comparators designed for several supply voltages.

## **Analog to Digital Converter**

**Definition:** Analog to digital converters are used where ever a peripheral generates analog input for a computer. The computer can only process data that is in digital form. The ADC converts from analog to digital. A temperature probe used for a science experiment might provide data that is to be displayed in graph form on a computer screen. The program that makes the graph processes a digital input signal to make the graph. The ADC converts the analog temperature data into the digital temperature data used for input by the computer.

**Availability:** From [www.analog.com](http://www.analog.com), I could find so many different types of ADC. I'll put only two different ADC to show how they explain their product.

**ADADC71 - Complete, High Resolution 16-Bit A/D Converters**



## ADADC85 - Fast, Complete 12-Bit A/D Converters

The ADADC85 devices are highspeed, low-cost 10- and 12-bit successive approximation analog-to-digital converters that include internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability ([www.analog.com](http://www.analog.com))

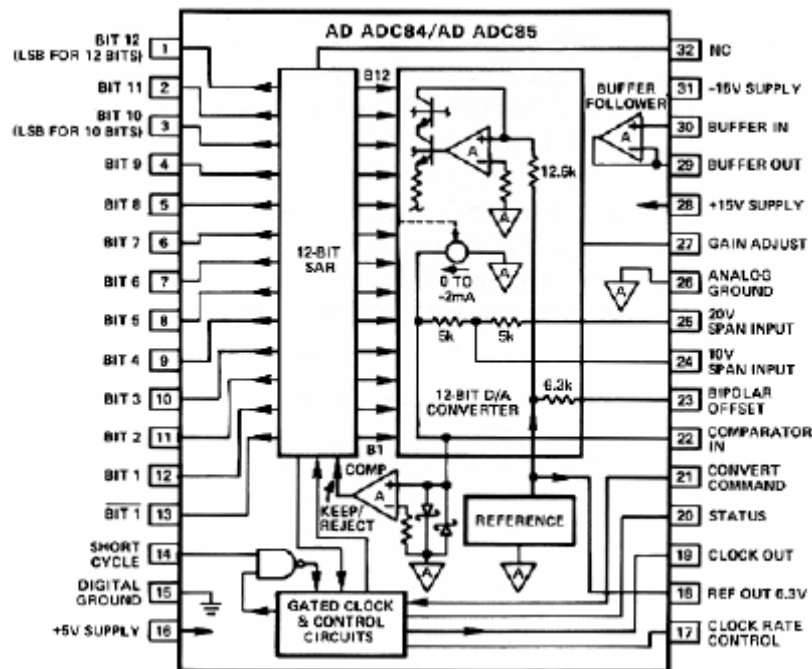


Figure 3 Functional Block Diagram

### Features

- Complete 12-bit A/D converter
- Fast successive approximation conversion: 10 $\mu$ s or 5 $\mu$ s
- Buried Zener reference for long-term stability and low Gain TC: 10ppm/C
- Max nonlinearity:  $\leq \pm 0.012\%$
- Low power: 880mW typical
- Chip count- high reliability
- Industry- standard pinout
- Z models for  $\pm 12$  V operation available
- MIL-STD-883B processing available
- Negative true parallel logic outputs
- Short cycle capability
- Precision +6.3V reference for external applications
- Price about \$200

## **Digital to Analog Converter (DAC)**

A digital to analog converter is a component that is used to derive or convert an analog signal from a digital signal. It is used in several applications. One of the most common applications is converting audio and sound signals. Analog to digital converters are one of the most common cells used in analog circuit design and is important in many applications of electrical engineering.

### **Conversion Time**

Conversion time is the time required by a digital to analog converter to full converter a digital input signal. This is important in circuit design because the longer the conversion time, the longer the delay in converting the signal and the slower the circuit will perform. These delays can also cause the circuit to not perform as expected.

### **Power Consumption**

Power consumption is the amount of voltage multiplied by the current ( $P=IV$ ). Not all cells will consume the same amount of power. It is desirable to have the least amount of power consumption as possible. By having lower power consumption, there is less risk at the chip over heating. It is also important not to waste power as once a full circuit is made, the power consumption of each

component in the circuit adds up. It is very challenging to make a chip that consumes a small amount of power.

### **Dimensions**

Dimensions is one of the most important parameters to consider when designing a cell. There are several advantages to having smaller dimensions in components in a circuit. Having smaller channel width to length ratios of the MOSFETs is advantageous as the current will have a shorter distance to travel and therefore, the MOSFET will operate faster. Other effects that need to be considered are parasitic and junction capacitance effects that can cause MOSFETs to slow down due to the charge build up that is developed. Optimizing dimensions is challenging and important.

### **Resolution**

Resolution is the amount of bits that are used in representing a digital signal. The higher the resolution, the more easily the original signal can be reconstructed. The number of bits that are used are  $(2)^n$ . The disadvantage of having a higher resolution is that the conversion time will take longer and hence, slow down the circuit. There is a trade off between resolution and speed of the digital to analog converter.

### **Sample Block Diagram**

Figure 4 shows a sample symbol for a DAC found on the AMI (Austria Micro Systems) website ([www.austriamicrosystems.com](http://www.austriamicrosystems.com)). The symbol shown here is the CDAC10\_C35. The CDAC10\_35 has a total of 23 pins and is a 10-bit digital to analog converter. It can run in two modes, which are the low swing mode and the high swing mode. Figures 5 and 6 show the diagrams for the configuration of low and high swinging mode, respectively. In low swing (LS) mode, VRES is shorted to VSSA and the output resistor RL is 25 ohms. The full scale output voltage at IOU TP and IOU TN should not exceed 0.625V. In high swing mode (HS), VRES is connected to VDDA and the output resistor RL is 50 ohms. The full-scale output voltage at IOU TP and IOU TN should not exceed 1.25V. In both cases, VBIASC must be left open. It is most suitable for applications requiring very high update rates and medium resolutions, such as direct digital synthesis, high-speed communications, and instrumentation. Typical applications include cellular base stations, digital microwave links, direct digital synthesis, arbitrary waveform generation, medical/ultrasound, high-speed instrumentation and control, and video/digital TV systems.

# SYMBOL

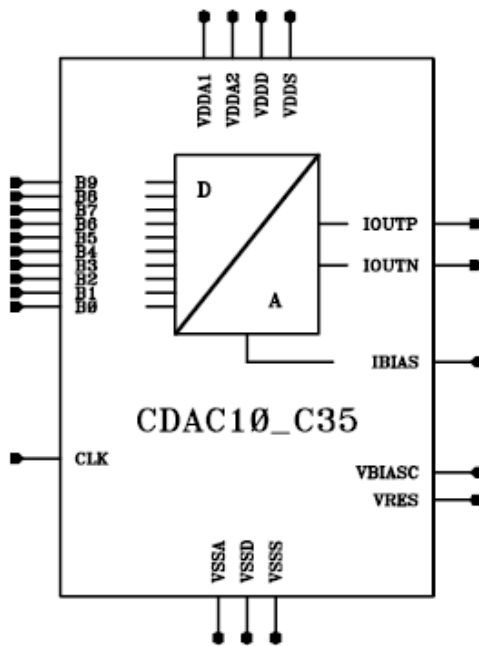


Figure 4 Symbol of CDAC10\_C35 Digital to Analog Converter

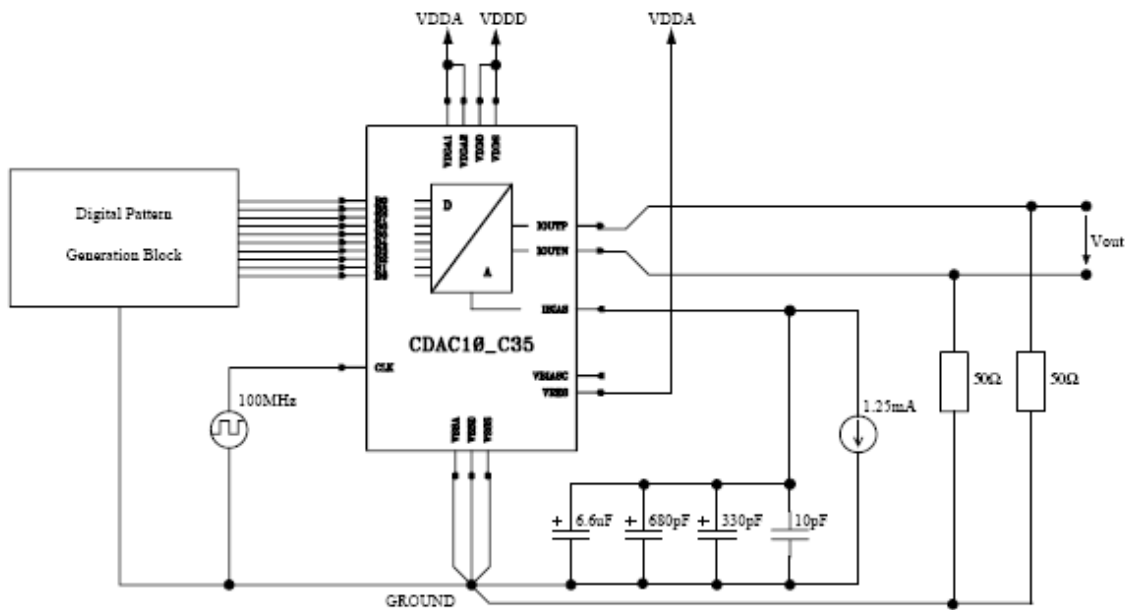
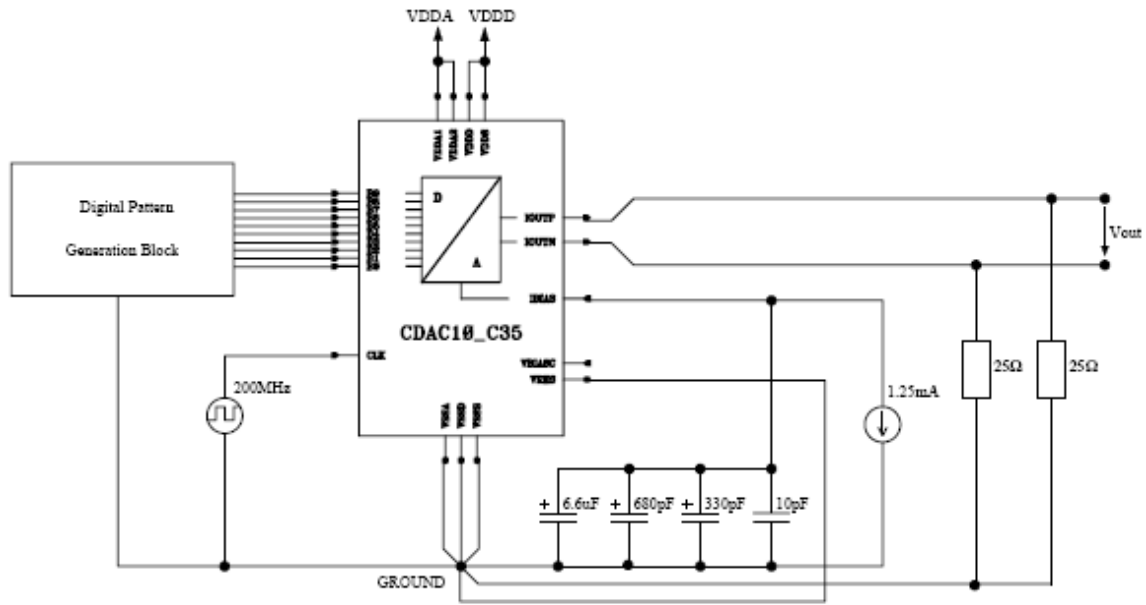


Figure 5 HS mode at fclk = 100MHz



**Figure 6 LS mode at fclk = 100MHz**

## Standard Cell Library

### Oklahoma State University VLSI

**A summary of the enhancements that Oklahoma State University cell library provides:**

- Freely available for all .edu sites
- Mailing list that provides access to all participants and instant news on possible enhancements and release dates for future generations of the library.
- Layouts of the leaf cells

- Characterized for delay and power. Area inserted into Synthesis file for possible area-sensitive synthesis runs.
  - Tutorials listed at this site that document step-by-step procedure for users aimed for student use.
  - Synopsys synthesis (.db) and Verilog/VHDL simulation libraries
  - Cadence TLF timing libraries
  - LEF files for the P&R tool
  - All abstracts from CDS' Abstract Generator
  - Various drive strengths.
  - Documentation that lists power, area, and speed for each device and technology.
  - Scripts that automate the procedure and are easy for students to use.
  - Scripts that automate insertion and simulation into public-domain and commercial tools.
  - Distribution enables Synopsys Design Ware (module compiler) components to be instantiated.
  - Verified through MOSIS multiple times with Pad Frame provided by MOSIS.
- Supported Technologies:**
- AMI 0.5um (with pad cells)

- AMI 0.35um (with pad cells)
- TSMC 0.25um
- TSMC 0.18um

**Provided files:**

- Timing Libraries: LIB, DB, TLF
- Simulation Libraries: Verilog, VHDL
- Geometry Libraries: LEF
- Cell layouts: Virtuoso, Magic

**Virginia Tech.**

The VTVT Group has developed a standard-cell library targeting the TSMC-0.25um, 2.5-volt CMOS process available via MOSIS. The library can be used with Synopsys synthesis tools and the Cadence Silicon Ensemble Place/Route tool. All of the cells can be viewed and edited using the Cadence Virtuoso layout editor. The cell library requires NCSU design kit or other kits that follow MOSIS design rules. Since MOSIS DEEP design rules are used for our cell library, the NCSU design kit has been modified slightly and is included in VTVT distribution

([http://www.ee.vt.edu/~ha/cell\\_library/distribution.html](http://www.ee.vt.edu/~ha/cell_library/distribution.html))

The package for our cell library includes:

- layouts of primitive cells

- Synopsys synthesis (.db) and VHDL simulation libraries
- LEF files for the PNR tool
- README file and a documentation for modification of the NCSU kit
- Other documentation, including the place and route flow we used to test the library.

Cell Name	Function
buf [1,2,4]	Noninverting buffer, drive strength 1, 2, or 4
inv [1,2,4]	Inverter, drive strength 1, 2 or 4
and2 [1,2,4]	2-input AND gate, drive strength 1, 2, or 4
and3 [1,2,4]	3-input AND gate, drive strength 1, 2, or 4
and4 [1,2,4]	4-input AND gate, drive strength 1, 2, or 4
or2 [1,2,4]	2-input OR gate, drive strength 1, 2, or 4
or3 [1,2,4]	3-input OR gate, drive strength 1, 2, or 4
or4 [1,2,4]	4-input OR gate, drive strength 1, 2, or 4
nand2 [1,2,4]	2-input NAND gate, drive strength 1, 2, or 4
nand3 [1,2,4]	3-input NAND gate, drive strength 1, 2, or 4
nand4 [1,2,4]	4-input NAND gate, drive strength 1, 2, or 4
nor2 [1,2,4]	2-input NOR gate, drive strength 1, 2, or 4
nor3 [1,2,4]	3-input NOR gate, drive strength 1, 2, or 4
nor4 [1,2,4]	4-input NOR gate, drive strength 1, 2, or 4
xor2 [1,2]	2-input XOR gate, drive strength 1 or 2
xnor2 [1,2]	2-input XNOR gate, drive strength 1 or 2
mux2 [1,2,4]	2-to-1 multiplexer, drive strength 1, 2, or 4
mux3 2	3-to-1 multiplexer, drive strength 2
mux4 2	4-to-1 multiplexer, drive strength 2
ABnorC	$(ip1*ip2+ip3)'$ , drive strength 1
ABorC	$ip1*ip2+ip3$ , drive strength 1
ab or c or d	$ip1*ip2+ip3+ip4$ , drive strength 1
not ab or c or d	$(ip1*ip2+ip3+ip4)'$ , drive strength 1
dec2 4	2 to 4 decoder, drive strength 1
dec3 8	3 to 8 decoder, drive strength 1
fulladder	One-bit ripple-carry adder, drive strength 1
bufzp 2	noninverting tristate buffer, low-enabled, drive strength 2
invzp [1,2,4]	inverting tristate buffer, low-enabled, drive strength 1, 2, or 4
cd 8	clock driver, drive strength 8
cd 12	clock driver, drive strength 12
cd 16	clock driver, drive strength 16
lp [1,2]	high-active D latch, drive strength 1 or 2
lrp [1, 2, 4]	high-active D latch with asynchronous low-active reset and drive strength 1, 2, or 4
lrsp [1, 2, 4]	high-active D latch with asynchronous low-active reset and asynchronous high-active set, drive strength 1, 2, or 4
dp [1,2,4]	rising-edge triggered D flip-flop (with 1, 2, or 4 drive strength)
drp [1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset (1, 2, or 4 drive strength)
drsp [1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset and asynchronous high-active set
dksp_1	rising-edge triggered D flip-flop with asynchronous active high set and extra inverted output.
dtsp_1	rising-edge triggered D flip-flop with asynchronous active high set input and serial scan input.
dtrsp_2	rising-edge triggered D flip-flop with asynchronous low-active reset, asynchronous high-active set, and serial scan input
jksp_2	rising-edge triggered JK flip-flop with asynchronous active-low reset and extra inverted output, drive strength 2.
filler	filler cell (empty cell with power and ground rails and nwell)

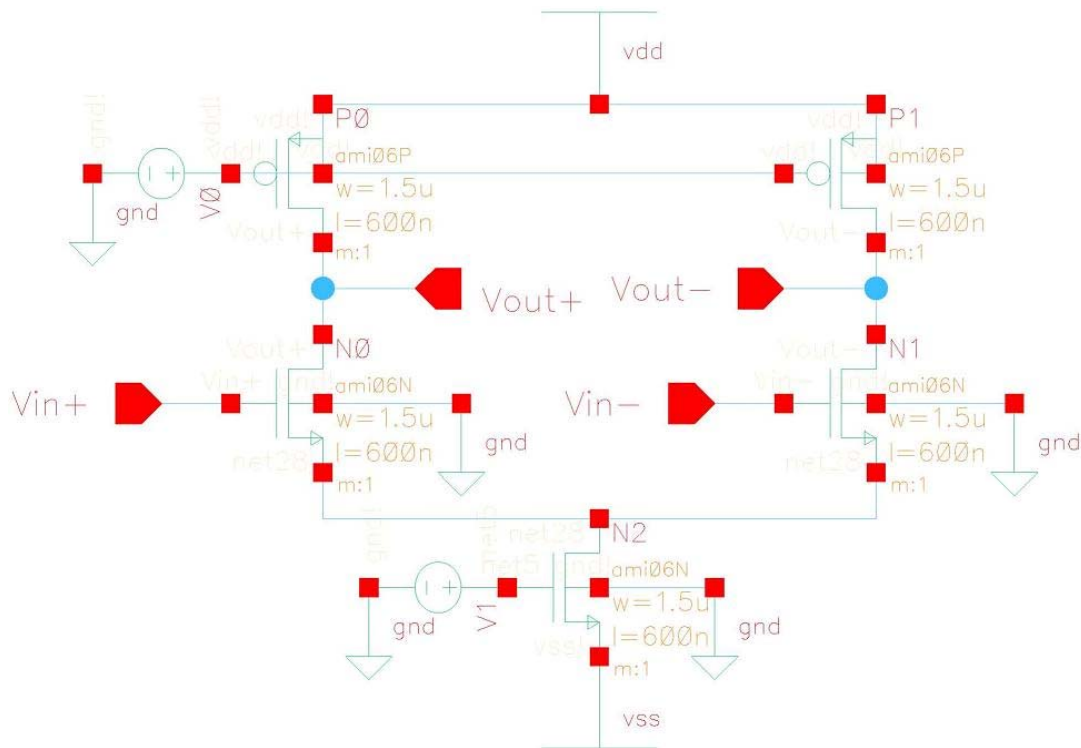
**Table 1 List of Cells Distributed**

## Design Work

Analog Cell Libraries are typically sold and packaged as a collection of symbols for a cad tool. Each symbol represents one cell, and the cell library user will have no knowledge of its internal workings (i.e., a schematic or layout). Instead, the cells will have a model attached that will let the user simulate their circuit as if the cell were actually there. The cell's real layout will be substituted in only at the fabrication stage.

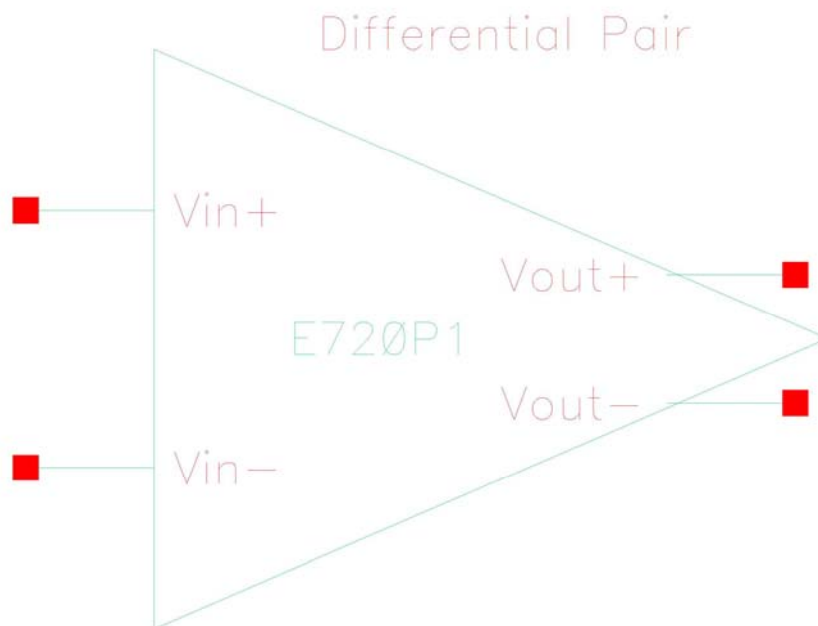
### Creating a Symbol using Cadence

In order for cell libraries to exist at all, it is essential that cad tools are able to support them. Therefore, it is important that symbols be used in circuits as well as created. To better illustrate the use of symbols in a cad tool, consider the fully differential amplifier located below as Figure 7.



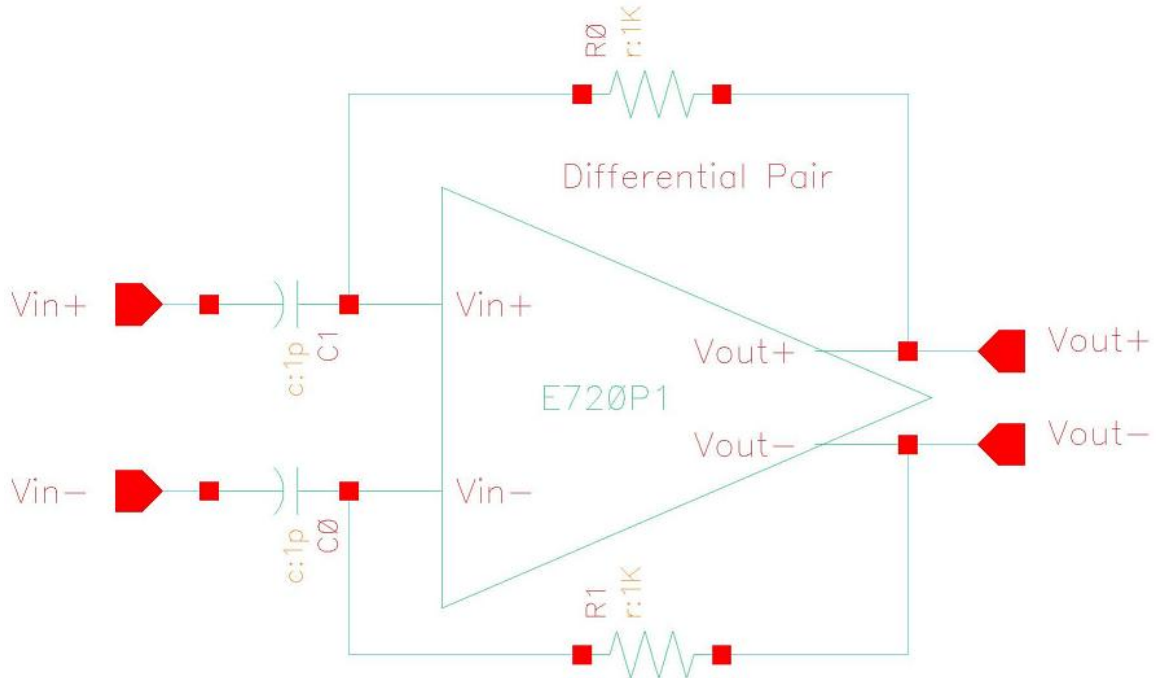
**Figure 7 A sample differential amplifier schematic**

The circuit in Figure 7 is a fully differential amplifier; it has two inputs ( $V_{in+}$  and  $V_{in-}$ ) and two outputs ( $V_{out+}$  and  $V_{out-}$ ). It is easy to create a symbol for this circuit in the cad tool Cadence. From the Virtuoso schematic editor, a stub can be generated using the *Create Cellview -> From Cellview* command. The stub contains a rectangle for the symbol as well as pins for the inputs and outputs. For the symbol to work correctly, the names of the input and output pins in the symbol must exactly match the ones used on the schematic. Next, the line tool can be utilized to change the shape that represents the symbol; for instance, it is convention to use a triangle to represent amplifiers, as shown in Figure 8.



**Figure 8 The differential amplifier symbol**

Finally, this symbol can now be used in place of the circuit just as any other library component, as shown in Figure 9.



**Figure 9: A circuit using the new differential amplifier symbol**

## Licensing Agreement

In addition to examining the cells from different cell libraries, the group also had the task of researching the process of licensing technology from companies such as Mosis for use in mixed cell library design. Because there is little documentation or standardization for analog cells, a large part of the task was simply finding someone who had information on this.

For the first part of research, the group contacted sales representatives from several fabrication companies, including AMI Semiconductor, IBM, and MOSIS. Group members explained that they were part of a research project to collect information on analog cell licensing, so that funding for a mixed cell library could be obtained. If funding could be secured, the students' professor would be interested in pursuing a fabrication and licensing agreement with an interested company. Unfortunately, the

reception by these companies was rather cold. Most companies failed to respond or expressed disinterest in aiding a student project without guaranteed funding. AMI Semiconductor did respond and asked for further information, but added that they do not have an analog cell library, only a few individual internal cells. While the group is continuing correspondence with AMI semiconductor, recent information from a company representative has cast doubt on the viability of this avenue. AMI seems quite reluctant to release information on its analog cells, mainly because they are internal cells rather than production cells. They have allowed a select few companies to have access to some of these cells, but only in the context of an existing fabrication deal that requires their use. AMI is also reluctant to give customer access to its website information without a fabrication or licensing contract. It seems that AMI will not be a useful source of information until the project has gained definite funding and a clearer idea of the kinds of cells that will be needed.

The group's other source of information is the standard, published licensing agreements posted on MOSIS' website. The first document studied was the confidentiality agreement between AMI and its customers. This document provided a great deal of information. First, it explained that AMI was at least partially owned by the MOSIS group, and that the licensing process seemed to be controlled by MOSIS. It also detailed exactly what is implied by "confidentiality." Effectively, the document said that any company licensing technology from AMI must agree to several terms. First, the technology and information licensed must be used only for the business relationship between AMI and the customer. This means that if AMI and the group were to set up a fabrication deal for a mixed cell library, then licensed cells from AMI could only be used

for that library, and not for any other projects. Second, the licensed technology may not be disclosed to another party, unless the party is employed by the customer and requires the information. In this case, the employee must likewise sign an equally restrictive confidentiality agreement. Third, any person signing such an agreement is obligated to report any unauthorized use of the licensed property directly to MOSIS. Fourth, customers are required to understand and obey applicable laws pertaining to the import and export of technology. Finally, once the project is over, all licensed technology and all copies must be returned to MOSIS.

The other available document is the AMI Design Kit Licensing Agreement, which explains conditions for customers using their design kit. First, the document explains that the design kit is available solely for use by customers who are seeking a hardware design deal with AMI. Second, the license agreement is valid only for the original purchaser; it is not transferable, exclusive, or available for sublicensing. Third, the agreement states that any modifications made by the customer and not by MOSIS could result in a hardware design that may be incompatible with the manufacturing process. Fourth, MOSIS or a subsidiary may discontinue part or all of its licensed technology, at which time MOSIS will inform the licensee. MOSIS retains full rights to modify, change, enhance, update, improve, or discontinue licensed technology. In addition to these conditions, several restrictions apply. MOSIS only permits storage and use of their licensed technology on the computers of the customer, at the customer's own facility. Also, the technology is to be used for internal design purposes only, and should not be manufactured or used in whole or in part by third parties. In the Delivery of Technology

section, MOSIS agrees that if the technology is not delivered properly and is lost or damaged as a result, they will replace it.

Another large section of the licensing agreement is Reproduction and Confidentiality.

There are a few important points in this section. First, it states that copying of the data is prohibited unless required by the licensee, and if copies are necessary, then they must be documented and kept by the licensee. Second, the agreement requires that all licensed technology be held by the licensee in strict confidence. Third, licensees are required to ensure that no one has access to the technology except for the licensee's employees that need such access. The licensee must take actions to ensure that such employees understand and comply with the agreement. Fourth, the agreement prohibits any efforts by the licensee or any other group to reverse-engineer the licensed technology. Possible consequences for violating this policy include termination of contract, court injunctions, and a lawsuit involving more than just money damages. Other sections include specifications for Limitation of Damages, Term, and Termination of the agreement.

## **Conclusion**

The purpose of this project was to gather information on licensing Intellectual Property as well as information on the current analog cell libraries currently being used in the industry. These analog cell libraries consisted of many different structures. Three of these major structures were chosen for discussion. The first structure that was discussed was the ADC. Examples and a discussion of the operation of an ADC were provided in this section. The next structure that was discussed was the DAC, which was discussed again in a similar manner as the ADC and the third section, the amplifiers. In each of these sections, the important parameters were defined as well as the trade off between

optimizing each parameter. The final section of the report discusses the correspondence between the group and MOSIS, AMI, and IBM for their pricing information and details about their current analog cell libraries.