

Team Asian Sensation

Presents...

ECE 683 Final Report

March 15, 2006

Jonathan Lee

Ke Sun

Lei Ma

Len Pan

Table of Contents

Executive Summary	3
Introduction.....	3
Background Research	3
Design Approach	4
Statement of Work	4
Resources	5
Schedule and Costs	5
Design Review Strategy.....	6
Introduction	7
Purpose.....	7
Problem Statement	8
Scope.....	8
Background Research	9
Design Approach	11
Statement of Work	12
Resources	14
Personnel.....	16
Facilities and Equipment.....	16
Schedules	17
Cost	17
Design Review Strategy	18
Sources Cited	20
Appendix A: Data Sheets	21
Appendix B: Netlists	29

Executive Summary

Introduction

A cell library is a collection of individual cells, which are blocks of transistors and connections that implement common logic functions or memory devices. For example, a single cell can refer to NAND gate or to a D flip-flop. The goal of the ECE 683 project is to conduct simulations to determine signal propagation delay for four new cells that were created during ECE 582. The final product will be a report that describes the project in detail, data from the simulations, and sets of equations and graphs that model the propagation delay.

Background Research

Research for this project was done for the simulation tools and methods to introduce propagation delay to the circuits. Cadence is the design tool used to design the cell schematic in ECE 582 and also provides tools for simulation. The major research components for ECE 683 consist of learning how to conduct simulations in Cadence, determining what parameter values to use, and how to present the information in a clear manner. Research was done on the Samsung library and MOSIS website to determine methods to introduce the two parameters into the circuits. The propagation delay is a linear equation in relation to both the capacitive loading and the input transition. From these libraries, the group learns that 3 different values for capacitive loading and input transition time are needed to accurately model the timing diagram.

Design Approach

For ECE 582, each group member chose a cell from the AO portion of the Samsung Cell Library and drafted a circuit design in Cadence. The cells were designed using complimentary CMOS (CCMOS), optimized for speed and size, and their logical operations were verified for correctness. For ECE 683, the design work is mostly limited to how to determine the most realistic propagation delay and how to present the data in an understandable way. The simulation data is based on two parameters, capacitive loading and input signal transition. Different quantities of these parameters produce different propagation delays for each circuit. Thus, each cell will have two graphs that show how the propagation delay is affected by each parameter. Other parameters used in the simulation, such as V_{dd} and transistor sizes, were chosen based on commonly used values.

Statement of Work

Two meetings were held with the customer to better understand the requirements and the ultimate result of the ECE 683 project. After getting a clearer picture, the team will determine what values for the many parameters are needed and learn how to simulate using Cadence. The major portion of the work consists of learning how to simulate propagation delay with Cadence, how to present the data in a useful manner, and actually producing a final report. The final report will contain a detailed description on how these simulations are performed and the results of the simulations.

Resources

The Cadence software suite has been provided by OSU free of charge and available on the computers in the Dreese UNIX lab. Other report work for this project was also done in the Caldwell lab.

Various online resources, primarily tutorials from OSU other universities, were used to learn about Cadence and different approaches to design and test cells. The Samsung cell library provided a resource on how to present propagation delay data.

An invaluable resource was the customer, Professor Steven Bibyk, who gave inputs and suggestions throughout the progress of the project.

Schedule and Costs

The schedule has been arranged in a way that leads up to the final goal of ECE 683, which is to have a report that summarizes the entire project. Since this project does not have any presentations and there is only one draft report, there are not a lot of important deadlines to follow.

The customer information sessions held at the beginning of the quarter gives the problem statement and clarifies the requirements of the project. Afterward, the team begins simulations, and a midway draft report was given to the customer to make sure satisfactory progress was being made. The final report provides the cell schematics, exact details of simulations, and the propagation delays.

There is no monetary cost associated with this project since Cadence is provided by the university and nothing physical has to be built. Time is the main constraint since the schematics and the report has to be completed within 10 weeks.

Design Review Strategy

Initially, the team only considered capacitive loading as the only major parameter that effected propagation delay. However, after an information session with the customer and looking at the Samsung cell library report, the team added signal transition time as another major parameter.

After halfway through the quarter, the team decided to report propagation delay for each parameter independent of the other parameter. The original plan was to combine the data from the two parameters and produce a three dimensional plot and a single propagation delay equation with two variables. However, after consulting with the customer, this format was judged to be not very helpful when users require a quick understanding of propagation delay for the four cells.

Introduction

Purpose

As more and more people find uses for digital devices, the demand for cheaper and more advanced VLSI chips will undoubtedly increase. Traditionally, the VLSI design phase has been a very resource intensive stage due to the difficulty of manually designing, placing, wiring, and optimizing the design. However, a standard cell-based design process can dramatically decrease the duration of this costly phase.

Standard cell-based design is a methodology that involves describing a chip's functionality using a hardware description language (HDL). The top-down methodology involves specifying the behavior of the chip and translating the specifications into a layout that is synthesized using a library of logic cells. Each logic cell encompasses the behavior of a common logic function or memory element, such as a logic gate or flip-flop. Today's VLSI chips may use hundreds of thousands of complex digital circuit components that can be described with a flexible HDL program such as VHDL or Verilog. Once the behavior of the chip has been described, other software tools, such as Cadence, can automatically synthesize, wire, and optimize the chip layout using the cell library.

Before a cell library can be used, designers must know some vital information about the library's components. A cell's propagation delay is a very crucial characteristic that designers must know. Propagation delay is the time difference between when the input starts to change and when a definite output is available.

Problem Statement

The Ohio State University Standard Cell Library (OSUSCL) is an ongoing academic project with the objective of making a viable cell library that can implement student designs while optimizing chip area and speed. While the current cell library can successfully implement elementary designs, there is still room for improvement. Adding additional cells that better describe common combinational logic functions and memory elements can further improve the flexibility and performance of the OSUSCL. However, if these new cells are to be optimally used, designers must know the propagation delay time. This specification for cells that were designed in ECE 582 is currently unknown, and thus renders these cells mostly useless from a chip design point of view.

Scope

The goal of this project is to provide propagation delay time for the AO211, AO21, OA32, and OA211 cells that were designed in ECE 582 in an easy to understand contribute format. The first major undertaking will be to learn how to conduct simulations in Cadence to find theoretical delay times. Afterward, the team will have to present the findings in a lucid format so designers can quickly know the propagation time for each cell. A final report will summarize in detail what the results are and how those results were acquired. This is the scope of what needs to be accomplished by the end of this quarter. The rest of this report will provide further detail on this project with Background Research, a Requirements Analysis, Design Approach, Statement of Work, Resources, and Schedule.

Background Research

Background research on simulation tools and methods to introduce propagation delay to the circuits was done for this project. The main tool to design the cell schematic in ECE 582 was Cadence which also provides tools for simulation. For ECE 683 the main research was done on learning how to conduct Cadence simulations, determining correct parameter values, and a clear manner to present the information. After two meetings with the customer, the team decided that a propagation delay is primarily based on two parameters: capacitive loading and input signal transition. The Samsung library and MOSIS website were overviewed to determine methods of introducing the two parameters into the circuits. The Samsung library uses a 3x3 grid to show how the propagation delay increases with capacitive loading and input signal transition. The MOSIS library uses a certain simple equation to describe the propagation delay for a capacitive load. From the equation, it shows that the propagation delay is a linear equation in relation to both the capacitive loading and the input transition. Using both of these techniques, the group can model the timing characteristic for each cell from a range of values for the capacitive loading and input transition.

From these libraries, the group learns that 3 different values for capacitive loading and input transition time are needed to accurately model the timing diagram. For the capacitive loading, 7 fF, 28 fF, and 350 fF can accurately model the propagation delay. 7 fF and 28 fF provide data that is close enough together to form a linear graph, and 350 fF is chosen to show how the propagation delay changes when the cell is cascaded with a more complex circuit. 100 ps, 400 ps, and 1000 ps are chosen for the input transition.

Those values provide a range of values that models the output from different types of cells.

All four group members are familiar with the basics of the Cadence environment. Each team member used the schematic designs from ECE 582 and implemented them again with capacitive loading and input transitions. The immediate customer for this project is Professor Steven Bibyk. These new cell schematics that are designed can be used as a learning tool for academia and possibly for commercial purposes. This report can also serve as an example for future ECE 683 classes.

Design Approach

For ECE 683, the goal is to obtain propagation delay results of certain cells. Each group member used the cell they built in ECE 582 and performed a set of simulations. After consulting with Professor Steven Bibyk, it was determined that two of the main factors that effect propagation delay are capacitive loading and input signal transition time. Practically speaking, the output of each cell would most likely be connected to additional circuitry, and the capacitance of this load could be represented by a single capacitor attached at the output node. The value of this capacitor was varied to analyze how capacitive loading effects propagation delay. A simple NAND or NOR gate² has a capacitance of approximately 7fF, so the values of the output capacitor chosen was multiples of 7fF. The convention used in simulations was to test the delay using a 7fF, 28fF, and 350fF capacitor. By using this convention, the results of different cells could be compared. The same approach was done when varying the input signal transition time. The rise and fall slopes used were 100ps, 400ps, and 1000ps. The transistor sizes are the default AMI 0.5um library size with the W/L set to 2/1 for the PMOS and 1/1 for the NMOS. The V_{dd} was set to 3V. For the simulation, only one transistor input was changed. This allowed for easier analysis of data on the output graph. To ensure that the worst case scenario for each cell was tested, the input transistor chosen was the part of the longest path from the output to the power rails.

The results of the data obtained was originally planned to be displayed in a 3D graph, but after further consideration it was decided that the results could be more easily be analyzed in multiple 2D graphs.

Statement of Work

In ECE 582, each team member designed a simple logic gate on the transistor level using Cadence. Afterwards, the design was tested to verify its functionality. For ECE 683, the delay characteristics of each cell were found.

First, Professor Bibyk met with the group to discuss the specifics of what he wanted for the project. After learning the objectives of the course, the group spent a week to learn how to do in-depth simulation using Cadence⁴. The team also did some basic background research by looking at existing university digital cell libraries and learned how Samsung characterizes the timing of their cells. The team found that there were two basic types of timing analysis. One form looked at only the propagation delay due to the load capacitance. The Samsung library performed a two variable timing analysis by considering both the load capacitance and the input slope. The team decided that the more to go with the more robust Samsung approach for this report.

After the second meeting with Professor Bibyk, the group performed the timing analysis on four cells using the Samsung method. After gathering the data, individual progress reports were sent to the customer to ensure the team was making satisfactory progress. After feedback on the results, data analysis is performed on the timing graphs to develop four graphs that show the trend line for the rise time and fall time due to load capacitance and input slope.

The last steps for the project involve performing a demonstration to the customer and writing this report. For the demonstration, the group will show the steps involved in the timing analysis of the cells, and answering any questions the customer may have⁶. A summary of the workflow is shown in Figure 1 below.

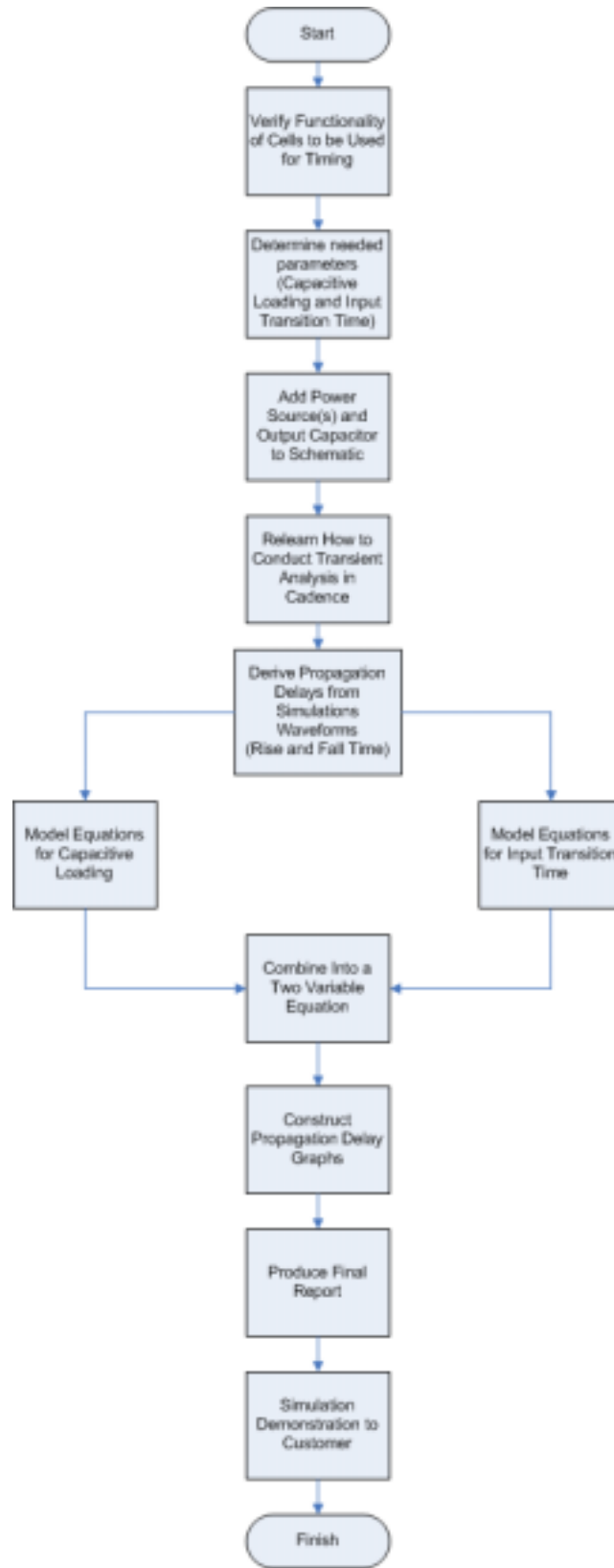


Figure 1: Project Workflow

A more detailed diagram of how the simulations were conducted is shown in figure 2. The only modification to the schematic from ECE 582 is adding in a capacitive load. Afterward, stimuli for the inputs are initialized. Essentially, the longest circuit path from input to output is chosen to determine the worst case propagation delay. A pulse with a rise and fall time transition is sent on the input for the longest path, and the results are plotted. From the plot, the rise and fall time delays are extracted using cursors and then finding the delta. The netlist for the simulation is saved⁵.

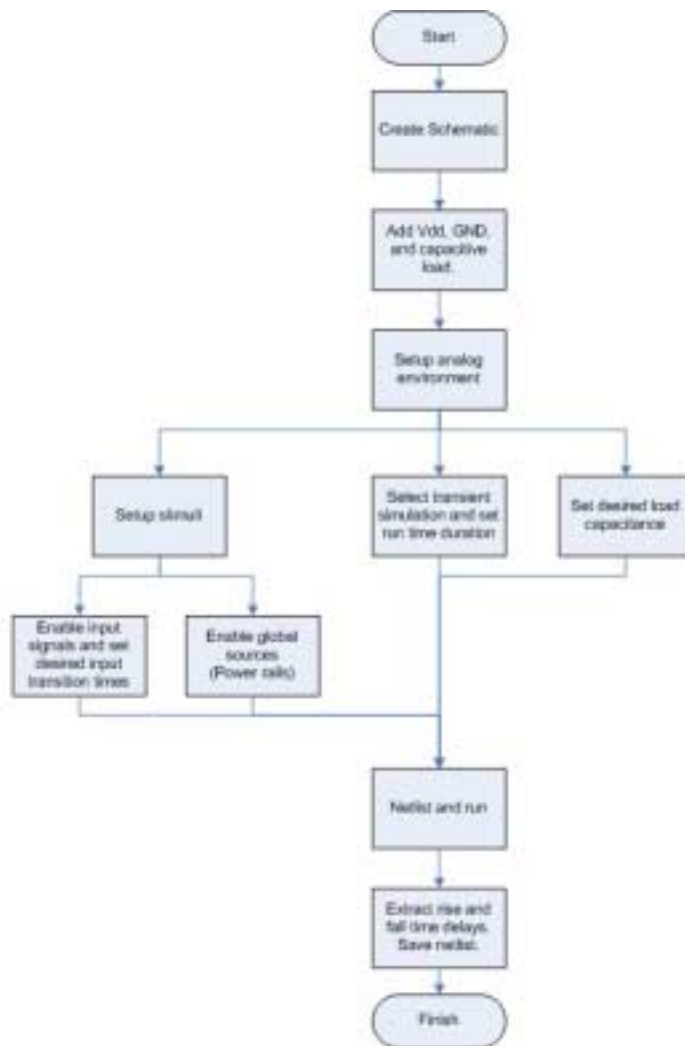


Figure 2: Obtaining Propagation Delays and Netlist

Propagation delays are obtained for three capacitances and three transition times, making a total of nine delay values for fall time and nine values for rise time. Three capacitive slope values are found based on keeping the transition time constant and increasing the capacitive load, and three transition time slopes are found for increasing transition times at each capacitive loads. The average of the first three slopes is the Average Capacitive Slope, and the average of the second three slopes is the Average Transition Time Slope. The variables used to model the propagation delay are the load capacitance and the input transition time. The equation also has a constant to compensate for any offset. The equation modeled is in the form:

$$\text{Propagation Delay} = (\text{Load Capacitance (fF)}) * (\text{Average Capacitive Slope}) + (\text{Rise/Fall Time (ps)}) * (\text{Average Transition Time Slope}) + \text{Constant}$$

Each individual simulation is run using a unique combination of load capacitance and input transition times. The constant can be calculated for each simulation since it is the only unknown in the equation. After calculating the constant for all nine simulations for the rise time, the average of these values is used to minimize error. The same procedure is done using the results from the fall time simulations to obtain the constant for the fall time propagation delay.

A template was created to calculate the Average Capacitive Slope, Average Transition Time Slope, and the Constant. The template used to find the equations that best model the propagation delay is seen in Appendix A. By double clicking on one of the worksheets in Appendix A, the propagation delays can be altered to model the delays of other cells. The propagation delays and delay equations for all four cells are listed in Appendix A.

Resources

Personnel

- **Jonathan Lee – Digital Logic Specialist**
- **Lei Ma – Report Editor**
- **Len Pan – Cadence Specialist**
- **Ke Sun – Timing Specialist**

Facilities and Equipment

All equipment and facilities for this project will be provided by the Ohio State University Electrical and Computer Engineering Department. The facility that will be used extensively will be the OSU's Electrical Engineering Dreese UNIX lab and the Caldwell PC lab. Almost all the computer work will be done in Cadence, Microsoft Word, Microsoft Visio, and Microsoft Paint.

Schedules

The proposed schedule follows the engineering design process and is open to changes as the project advances. Table 1 includes a proposed project schedule for this quarter. The Project Introduction phase motivates the group to start thinking critically about the requirements of the project and is followed by the Learn Simulation in Cadence phase. This phase involves relearning certain aspects of Cadence and how to conduct simulations to find propagation delay. Afterward, the actual simulations will be conducted and Sample Reports will be written up to make sure the customer is satisfied with the results. Feedback from the Sample Reports will be given at the Midway Review, which is followed by Data Analysis. After getting feedback on the sample report, the team can start the Final Report. A Demonstration will be given to the customer to ensure that the process used to obtain the data is valid. The Final Report will be submitted on March 15, 2006.

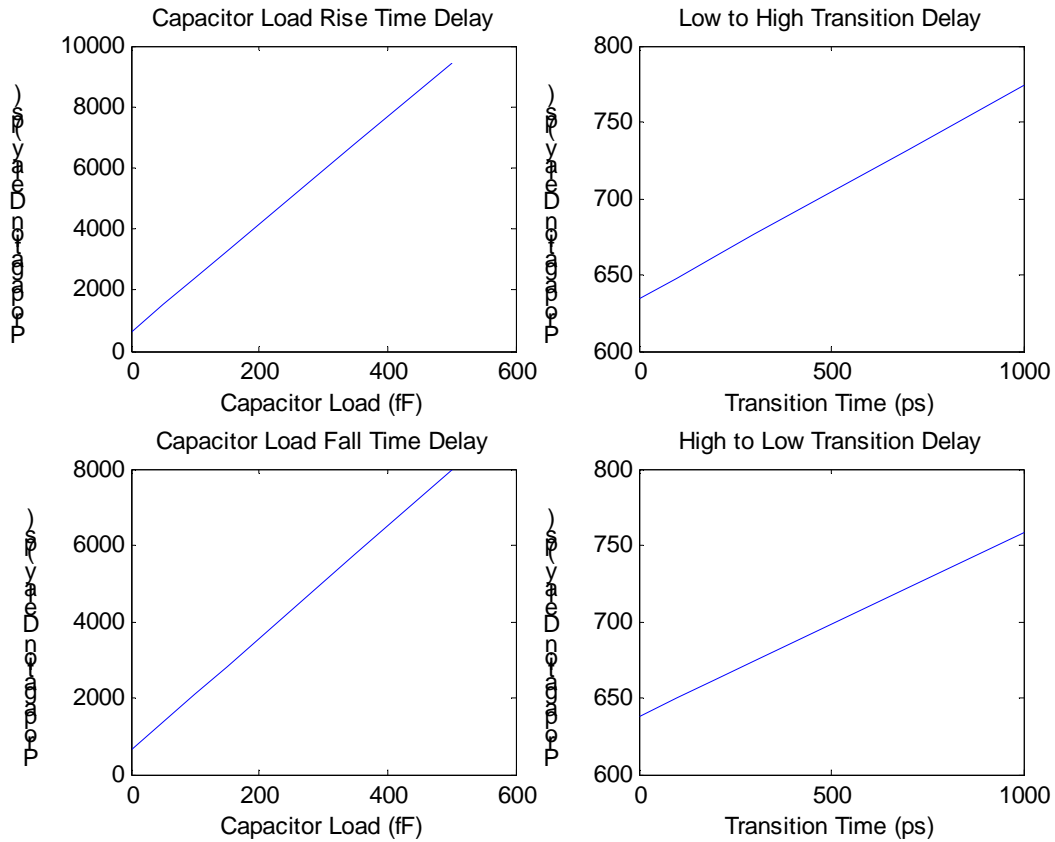
ID	Task Name	Start	Finish	Duration	Jan 2006			Feb 2006			Mar 2006					
					1/1	1/8	1/15	1/22	1/29	2/5	2/12	2/19	2/26	3/5	3/12	
1	Project Introduction	1/9/2006	1/16/2006	6d	[Gantt bar from 1/9 to 1/16]											
2	Learn Simulation in Cadence	1/16/2006	1/25/2006	6d	[Gantt bar from 1/16 to 1/25]											
3	Conduct Simulations	2/1/2006	2/6/2006	4d	[Gantt bar from 2/1 to 2/6]											
4	Sample Reports	2/15/2006	2/22/2006	6d	[Gantt bar from 2/15 to 2/22]											
5	Midway Review	2/27/2006	2/27/2006	1d	[Gantt bar at 2/27]											
6	Data Analysis	2/28/2006	3/2/2006	3d	[Gantt bar from 2/28 to 3/2]											
7	Demonstration	3/8/2006	3/8/2006	1d	[Gantt bar at 3/8]											
8	Final Report	2/27/2006	3/15/2006	13d	[Gantt bar from 2/27 to 3/15]											

Table 1. *Proposed project schedule*

Cost

Since all facilities and software packages will be provided The Ohio State University, there will be no monetary costs associated with this project.

found the propagation delay due to the capacitor load. The second graph found the propagation delay due the rise transition time. The same two graphs were then made for the fall times. A sample graph is included below.



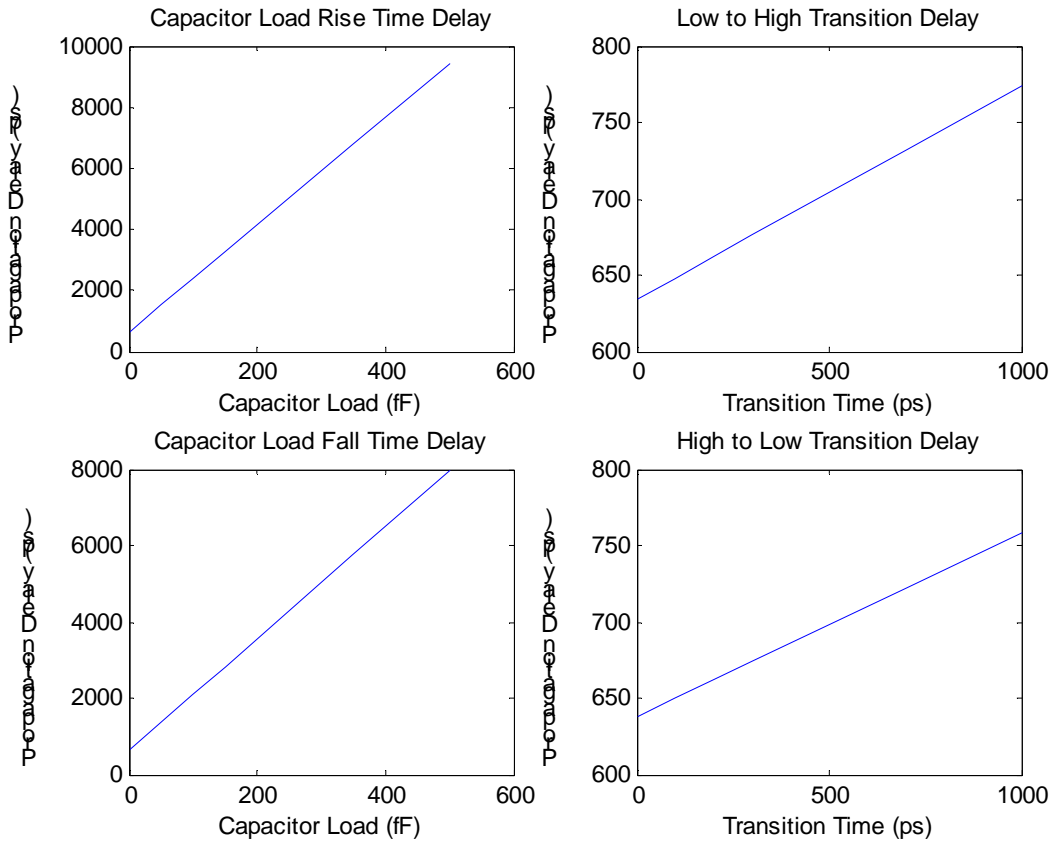
As expected, the propagation delay grew linearly with respect to both the load capacitance and the rise/fall transition times. The propagation delay was longer for circuits that had several transistors in series since the circuit had to charge a larger capacitance. The error of the calculated to theoretical values was pretty small. The largest error found was around 5%.

Sources Cited

- [1] Brian Dupaix, “STD90/MDL90 0.35m 3.3V CMOS Standard Cell Library for Pure Logic/MDL Products”, The Ohio State University
- [2] J. Copus, “Open Digital HDL to Synthesized Layout Flow for Mixed Signal IC’s,” M.S. Thesis, The Ohio State University, Columbus, OH, United States, 2003.
- [3] A. Sedra and K. Smith, "Microelectronic Circuits", 5th Edition, Oxford University Press, 2003, Chapter 10
- [4] Department of Electrical Engineering, The Ohio State University, “Cadence Central”, www.ece.osu.edu/cadence <http://www.ece.osu.edu/cadence/>
- [5] Cadence University Program Member, University of Virginia, “CADENCE Tutorials”, Oct 24 2005, www.ee.virginia.edu/~mrs8n/cadence/Cadencetutorials.html
- [6] G. Hafezi, “How to Start with Cadence”, The Ohio State University, Columbus, OH, United States, 2005

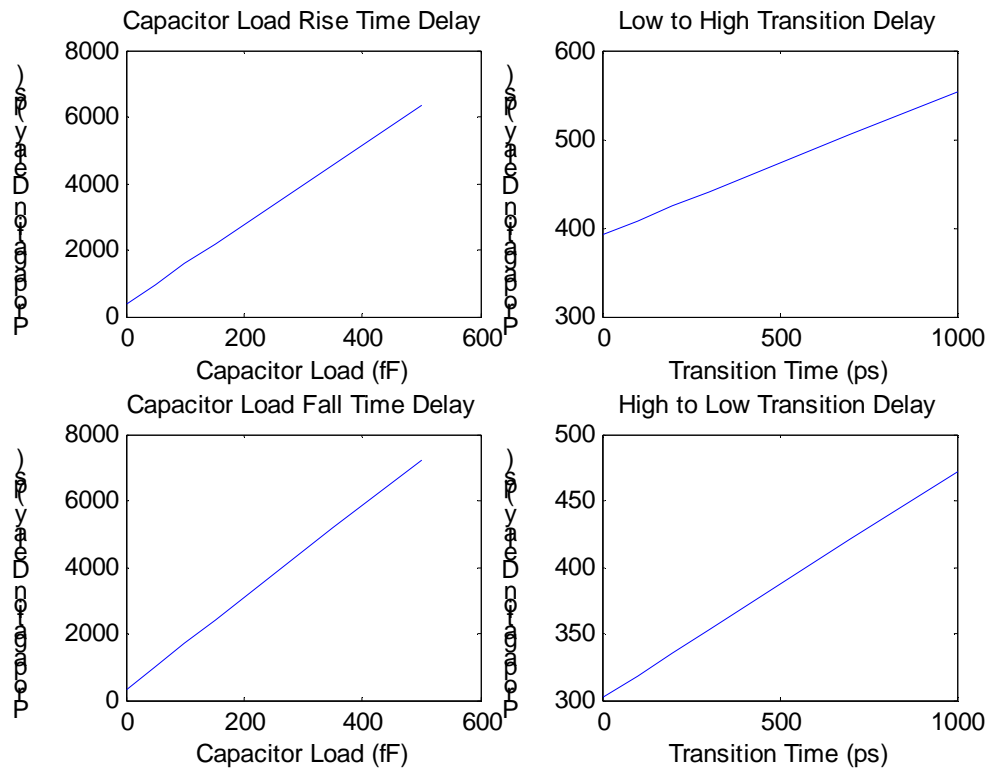
$$RiseTimePropagationDelay = 17.54(CapacitorLoad) + 0.14(RiseTransTime) + 634.05$$

$$FallTimePropagationDelay = 14.68(CapacitorLoad) + 0.12(FallTransTime) + 637.85$$



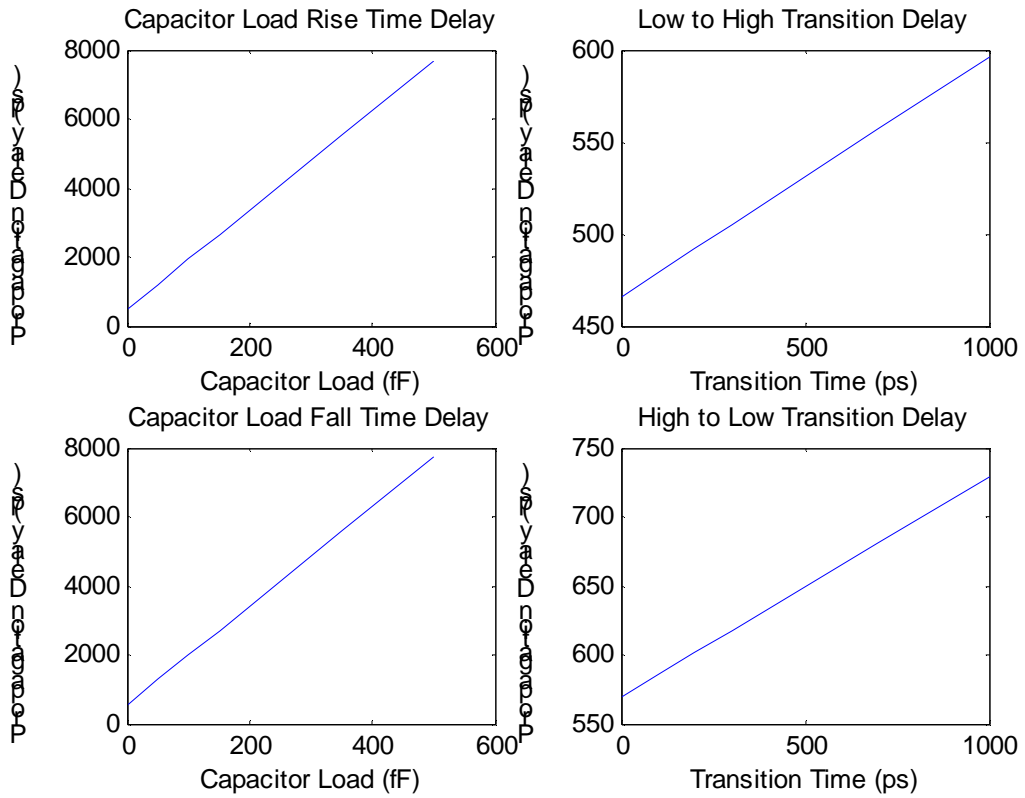
$$RiseTimePropagationDelay = 11.86(CapacitorLoad) + 0.16(RiseTransTime) + 392.5$$

$$FallTimePropagationDelay = 13.88(CapacitorLoad) + 0.17(FallTransTime) + 301.5$$



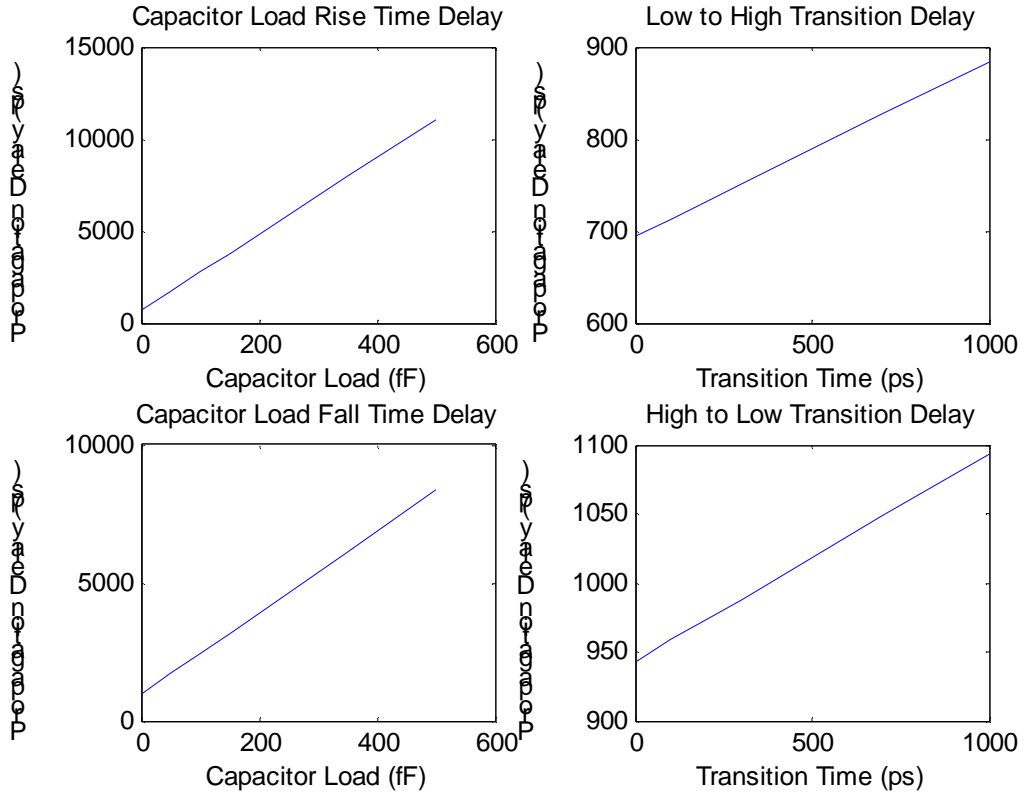
$$RiseTimePropagationDelay = 14.47(CapacitorLoad) + 0.13(RiseTransTime) + 466.2$$

$$FallTimePropagationDelay = 14.36(CapacitorLoad) + 0.16(FallTransTime) + 569.6$$



$$RiseTimePropagationDelay = 20.73(CapacitorLoad) + 0.19(RiseTransTime) + 693.8$$

$$FallTimePropagationDelay = 14.88(CapacitorLoad) + 0.15(FallTransTime) + 943.2$$



Appendix B: Netlists

```
// Generated for: spectre
// Generated on: Mar 15 10:54:18 2006
// Design library name: Lei_test_lib
// Design cell name: ao211
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include
"/opt/local/cadence/IC5033_usr3/tools.hppa/dfII/samples/artist/ahdlLib/
quantity.spectre"
include
"/opt/local/cadence/design_kits/NCSU/current/local//models/spectre/nom/
allModels.scs"

// Library name: Lei_test_lib
// Cell name: ao211x1
// View name: schematic
C0 (Y 0) capacitor c=28f m=1
P3 (Y D net11 vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u
pd=9u \
    m=1 region=sat
P2 (net11 C net20 vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u
\
    pd=9u m=1 region=sat
P1 (net20 B vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
    pd=9u m=1 region=sat
P0 (net20 A vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
    pd=9u m=1 region=sat
N3 (Y D 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u
m=1 \
    region=sat
N2 (Y C 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u
m=1 \
    region=sat
N1 (net32 B 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
N0 (Y A net32 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
```

```

// Generated for: spectre
// Generated on: Mar 15 10:42:33 2006
// Design library name: test
// Design cell name: ao21
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include
"/opt/local/cadence/IC5033_usr3/tools.hppa/dfII/samples/artist/ahdlLib/
quantity.spectre"
include
"/opt/local/cadence/design_kits/NCSU/current/local//models/spectre/nom/
allModels.scs"

// Library name: test
// Cell name: ao21
// View name: schematic
C0 (Y 0) capacitor c=350f m=1
P2 (Y B net035 vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u
pd=9u \
    m=1 region=sat
P1 (Y A net035 vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u
pd=9u \
    m=1 region=sat
P0 (net035 C vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u
\
    pd=9u m=1 region=sat
N2 (net23 B 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
N1 (Y C 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u pd=6u
m=1 \
    region=sat
N0 (Y A net23 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat

```

```

// Generated for: spectre
// Generated on: Mar 15 10:59:07 2006
// Design library name: leejo_ami06
// Design cell name: oa32
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include
"/opt/local/cadence/IC5033_usr3/tools.hppa/dfII/samples/artist/ahdlLib/
quantity.spectre"
include
"/opt/local/cadence/design_kits/NCSU/current/local//models/spectre/nom/
allModels.scs"

// Library name: leejo_ami06
// Cell name: celleecap
// View name: schematic
C0 (vout 0) capacitor c=28f m=1
N7 (net1 vd 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
N6 (net070 net1 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
N5 (net9 net070 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
N4 (vout net17 net9 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12
ps=6u \
    pd=6u m=1 region=sat
N3 (net17 net33 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
N2 (net33 vc 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
N1 (net33 vb 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
N8 (net1 ve 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
N0 (net33 va 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
pd=6u \
    m=1 region=sat
P8 (vout net070 vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
\
    ps=6u pd=6u m=1 region=sat
P7 (vout net17 vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
\
    ps=6u pd=6u m=1 region=sat
P6 (net17 net33 vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
\
    ps=6u pd=6u m=1 region=sat
P5 (net070 net1 vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
\
    ps=6u pd=6u m=1 region=sat

```

```
P4 (net1 ve net56 vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
ps=6u \
    pd=6u m=1 region=sat
P3 (net56 vd vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
ps=6u \
    pd=6u m=1 region=sat
P2 (net33 vc net64 vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \
ps=6u pd=6u m=1 region=sat
P1 (net64 vb net68 vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \
ps=6u pd=6u m=1 region=sat
P0 (net68 va vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
ps=6u \
    pd=6u m=1 region=sat
```

```

// Generated for: spectre
// Generated on: Mar 14 20:30:22 2006
// Design library name: kelib
// Design cell name: oa211
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include
"/opt/local/cadence/IC5033_usr3/tools.hppa/dfII/samples/artist/ahdlLib/
quantity.spectre"
include
"/opt/local/cadence/design_kits/NCSU/current/local//models/spectre/nom/
allModels.scs"

// Library name: kelib
// Cell name: mycell
// View name: schematic
C0 (Y 0) capacitor c=350f m=1
P5 (Y V_D vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
P4 (Y V_C vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
P3 (Y net86 vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
ps=6u \
    pd=6u m=1 region=sat
P2 (net69 V_A vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12 \
    ps=6u pd=6u m=1 region=sat
P1 (net94 V_B net69 vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
\
    ps=6u pd=6u m=1 region=sat
P0 (net86 net94 vdd! vdd!) ami06P w=1.5u l=600n as=2.25e-12 ad=2.25e-12
\
    ps=6u pd=6u m=1 region=sat
N5 (net74 V_D 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
    pd=6u m=1 region=sat
N4 (net78 V_C net74 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12
ps=6u \
    pd=6u m=1 region=sat
N3 (Y net86 net78 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
N2 (net86 net94 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u
\
    pd=6u m=1 region=sat
N1 (net94 V_B 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
    pd=6u m=1 region=sat
N0 (net94 V_A 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
    pd=6u m=1 region=sat

```