

The Ohio State University
Department of Electrical and Computer Engineering

ECE 261

Introduction to Logic Design

Winter 2009

Meeting Time: 4:30 pm MWF, 1015 McPherson Lab
Instructor: Professor David Orin, 660 Dreese Labs
Office Hours: 9:30 am MW
Grader: Arjun Penumatsa, penumatsa.1@osu.edu
ECE206 TAs & Office Hrs: Amneh Akour, akour.1@osu.edu, 10:30-11:30 Tues, 12-2 Wed, 303CL
Yalcin Balcioglu, balcioglu.1@osu.edu, 2-5 pm Tues, 805DL
Rong Yang, yang.1147@osu.edu, 9:30-11:30 Mon, 10-11 Fri, 234CL
Course Website: <http://www.ece.osu.edu/~orin/ece261>
Text: *Logic and Computer Design Fundamentals*, 4th Ed.,
by M.M. Mano & C.R. Kime
Reference: *Digital Design: Principles & Practices*, 4th Ed., by J.F. Wakerly
Prerequisites: Math 152, Physics 132, En Graph 167 or CSE 202 or CSE 221
Computer Projects: Using Xilinx on PCs running Windows XP
Xilinx Software Support: Bea Jarupan, 600DL
<http://www.ece.osu.edu/xilinx>
Grades Via Carmen: <http://carmen.osu.edu>

Grading:	Quizzes	12%
(Tentative)	Computer Projects & Homeworks	18%
	Midterm Exams (2)	40%
	Final Exam	30%

Computer Projects

During the quarter, three computer projects will be assigned and graded. These projects will use the Xilinx software distributed with the book. The Department operates a PC lab with Xilinx software installed, and students may also use their own computers to execute designs. If you are going to use your own computer, be sure to download and install the latest software WebPACK from Xilinx.

The projects are designed to reinforce concepts learned in class, to allow you to better understand the characteristics of circuits studied in the course by simulating them, and to increase your exposure to CAD software in general. Bea Jarupan is available to work with students on these and other Xilinx projects. She will serve as your primary contact for questions concerning the Xilinx software.

General Comments

1. There will be short quizzes (about ten minutes) most Wednesdays. The lowest quiz grade will be dropped. As a result, there will be **no make-up quizzes**.
2. Homeworks will be assigned most weeks. They will typically be due on the following Wednesday in class. **No late homeworks** will be accepted. The lowest homework grade will be dropped. Solutions will be made available on Carmen after the due date for the assignment.
3. All exams and quizzes will be closed book and notes and no calculators. One week's notice will be given to announce the day of each midterm exam. Make-up exams will virtually NEVER be given.
4. Grading questions must be resolved within one week of the time when the graded work is returned. Check with the grader first and then with the instructor as needed.
5. Computer projects will be completed in groups of two or three, with one report turned in per group.
6. You are responsible for all the assigned sections in the text and course materials and all lecture content unless otherwise specified by the instructor. If you miss class, it is your responsibility to obtain assignments and other information given on the days you missed.

Goals

The principal goal of this course is to provide an introduction to digital logic design which is the basis for computer hardware development. The student should, at the completion of the course, be able to analyze and design logic circuits by understanding formal foundations and selected design techniques.

Eta Kappa Nu (HKN) Peer Mentoring

This is a FREE TUTORING service for ECE students like you! Please come take advantage of this opportunity to ask questions, learn, and interact with your peers.

Location: Caldwell 267

Hours: The tutor room is open during regular work hours, with some variability due to individual tutors' schedules and course loads. Specific times can be found on OSU's HKN website: <http://www.ece.osu.edu/hkn/>.

Class Schedule (Tentative)

Day	Reading	Subject	Problems
1	1-1, 2	Digital systems & information, number systems	1-4, 8, 9*, 10*, 11*
2	1-3, 4	Arithmetic operations, decimal codes	1-12, 13, 19*
3	1-5, 6, 7	Alphanumeric codes, gray codes	1-22, 23, 25*, 26
4	2-1	Combinational logic circuits, binary logic and gates	2-1*
5	2-2	Boolean algebra	2-2*a,b,c, 6b,c,d,e, 7*, 9*
6	2-3	Standard forms	2-10*, 11, 13c
7	2-4	Two-level circuit optimization	2-15*, 16, 17
8	2-5	Map manipulation	2-19*, 20, 22*, 23, 24, 25*, 26
9	2-8, 9, 10, 11	Other gate types, exclusive-OR operator and gates, high-impedance outputs	2-34
10		Review	
11		Midterm 1	
12	3-1, 2	Combinational logic design, design procedure, beginning hierarchical design	3-1, 2*, 3, 8, 9, 10, 11a
13	3-3, 4	Technology mapping, verification	3-15, 16, 17, 20
14	3-5, 6	Combinational functional blocks, rudimentary logic functions	
15	3-7, 9, 10	Decoding, multiplexers	3-28, 33, 37
16		Decoder/multiplexer-based combinational circuits	3-44, 46, 48
17	4-1, 2	Arithmetic functions, iterative combinational circuits, binary adders	4-2*
18	4-3, 4	Binary subtraction, binary adder-subtractors	4-3*, 4, 5, 6*, 7, 8, 16*
19	5-1, 2	Sequential circuits, latches	5-2
20	5-3	Flip-flops	
21	5-4	Sequential circuit analysis	5-6, 7*, 8, 9, 10, 11*
22		Review	
23		Midterm 2	
24	5-5	Sequential circuit design	5-13*, 14, 18*, 19, 22
25		More sequential circuit design	5-25, 27*, 28a,b
26	5-6	Other flip-flop types	
27	7-1	Registers and load enable	
28	7-6 c	Shift registers	7-6*, 7a,b
29	7-6 d,e,f	Counters	7-8, 14*, 15
30		Review for final	

* Practice problems that do not need to be turned in for grading. Solutions for these are available on the companion website for the textbook.