

ECE 561: Digital Circuit Design

Homework #1

Problems:

1. Show how to build a flip-flop equivalent to the 74x109 positive-edge-triggered $J\text{-}\overline{K}$ flip-flop using a 74x74 positive-edge-triggered D flip-flop and one or more gates from a 74x00 package. Hint: note the characteristic equation for a J-K flip-flop.
2. Problem 7.18. Also draw a state diagram.
3. Problem 7.19.
4. Problem 7.21c. Note that a state diagram is ambiguous if “mutual exclusion” and “all inclusion” are not satisfied for the transitions out of each state. See the discussion in the text on pg. 553.