

# ECE 561: Digital Circuit Design

## Homework #2

### Problems:

1. Consider you are far off in Timbuktu and you have burned out your last J-K flip-flop (from a 74LS112 package). But all is not lost – you have one D flip-flop (from a 74LS74 package), and altogether the following spare gates (not packages) on your board: one Inverter (74LS04 package), one two-input OR gate (74LS32 package), and two two-input NAND gates (74LS00 package). Note that the 74LS112 J-K flip-flop is similar to a 74LS109 J- $\bar{K}$  flip-flop except that it has a high activated K input and is triggered by a high to low transition of the input clock.
  - (a) Using the available devices, design a circuit which will replace your burned out J-K flip-flop (falling edge-triggered). Using proper symbology, draw the resulting logic diagram. (Note: the Inverter must be used to tie the system clock,  $SYSCLK-$ , to the CLK on the flip-flop.)
  - (b) Given the propagation delay values in Table 6-2 (pg. 366 of text) and Table 8-1 (pg. 684 of text), what are the setup and hold times for J and for K of your new flip-flop? What is the maximum clock frequency for the new flip-flop? Note: to simplify the problem, just use the “Maximum” values from the tables.
2. Problem 8.13. Note that  $RCO$  is active low and has the following function:
$$RCO = ENT \cdot (UP/DN \cdot QD \cdot QC \cdot QB \cdot QA + \overline{UP/DN} \cdot \overline{QD} \cdot \overline{QC} \cdot \overline{QB} \cdot \overline{QA})$$
3. Problem 8.14.
4. Problem 8.35. Change the count sequence in the problem to:  
3, 4, 5, ..., 12, 13, 3, 4, 5, ...
  - (a) First design the modulo-11 counter with the 74x163 and a minimum number of NANDs and INVERTERS.
  - (b) Then design the modulo-11 counter with the 74x163 and a 74x138 decoder.
5. Problem 8.38. Change the problem to allow for an additional inverter.
6. Problem 8.55. Use a 74198 and 74LS30.