

ECE 561: Digital Circuit Design

Homework #3

Problems:

1. (a) Use the three-step approach to analyze the first circuit on the following page (equations, transition/excitation state table, and state diagram). Keep the state in numeric (non-symbolic) form. Assume that only three bits of the counter are used.
(b) What is the maximum system clock frequency? Be sure to show the critical path. Use the timing specifications for the 74LS04, 74LS08, and 74LS139 from Tables 6-2 and 6-3, pp. 366-7 in the text (“Maximum” columns) and the specs for the 74LS163 (or 74LS161) as given in class for the two’s complement example.
2. (a) Use the three-step approach to analyze the *System Controller* in the second circuit on the following page. Note that only two bits of the counter are used. Be sure to finish with a state diagram with all inputs and outputs clearly marked (with numeric coding for the states).
(b) Repeat Part (a) for the entire circuit.
(c) Calculate the maximum frequency for the entire circuit using these additional specifications for the 74LS109:

t_{pLH}	25 ns	(includes CLR & PR $\rightarrow Q, \bar{Q}$)
t_{pHL}	40	"
t_s	35	
t_h	5	

Indicate the critical path.

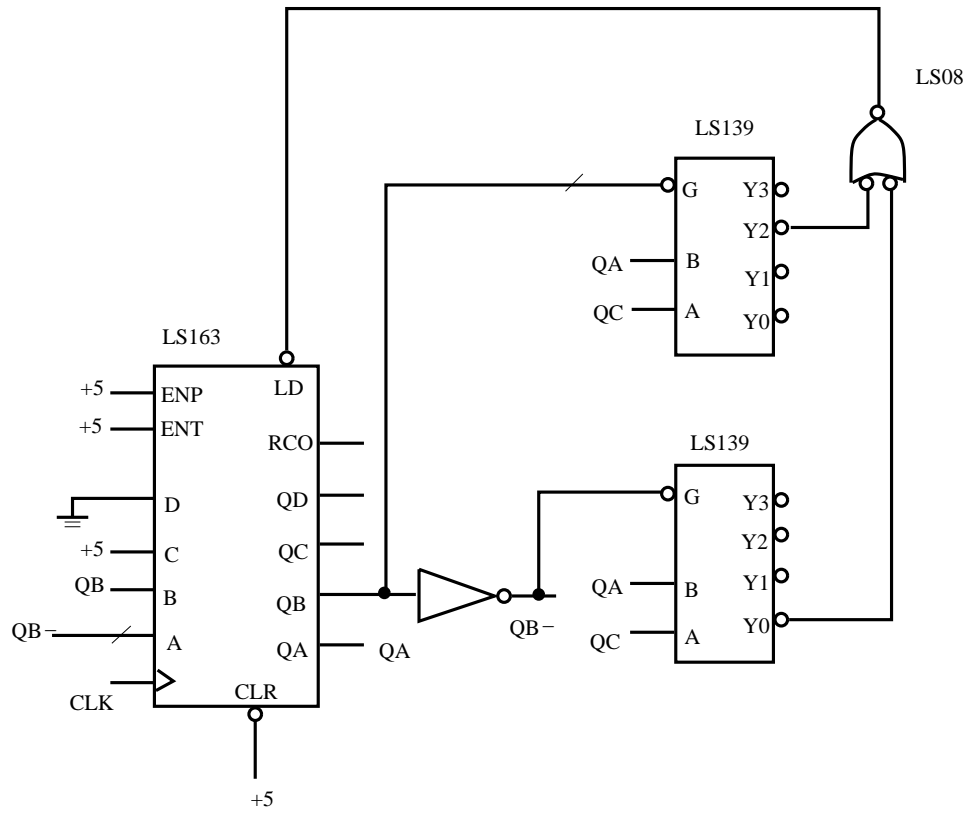


Figure 1: Problem 1.

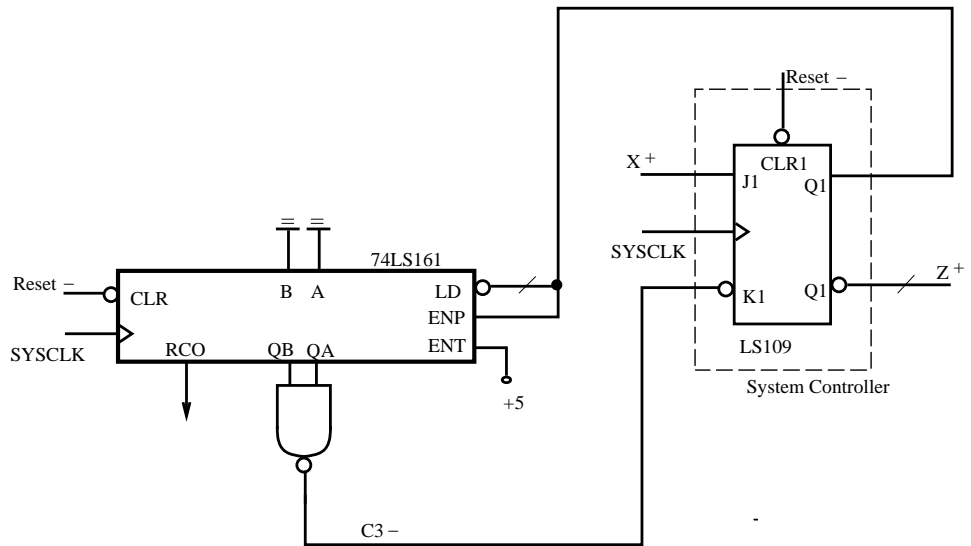


Figure 2: Problem 2.