

ECE 561: Digital Circuit Design

Homework #4

Problems:

1. Problem 7.44. Assume that once INIT is negated, it will not be asserted again until sometime after Z goes to a 1.
2. Design a clocked synchronous state machine that checks a serial data line for even parity. The circuit should have two inputs, SYNC and DATA, in addition to CLOCK, and one Moore-type output, ERROR. Devise a state/output table that does the job using just four states and include a description of each state's meaning in the table. *No other steps need to be completed.*

Note Figure 2-16 on pg. 69 of the text for the basic concepts of serial data transmission. Assume that ERROR is asserted during the transmission of bit 2 if the previous byte had odd parity. It remains asserted for eight clock periods.
3. Problem 7.51. Use two state variables, Q_1Q_0 , with the state assignment A0=00, A1=01, OK0=10, and OK1=11.
4. Problem 7.52.