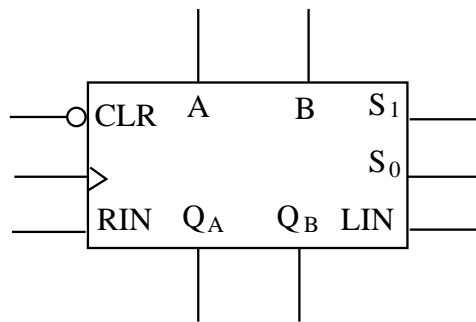


ECE 561: Digital Circuit Design

Homework #5

Problems:

- (a) Use the 9-step design approach to design a 2-bit version of the 74LS194 with NAND gates ('LS00, 'LS10, ...), inverters ('LS04), and D flip/flops (74LS74). You need not provide a state diagram in this case but be sure to finish with a complete logic diagram. Use the following block diagram:



- (b) Use the timing specifications from Table 6-2 in the text ("Maximum" values) for the gates and from Table 8-1 for the 74LS74 to provide similar specifications for the 2-bit shift register:

Two-Bit Shift Register:

$$\begin{aligned}
 t_s & S_1, S_0 \\
 & B, A \\
 & RIN, LIN \\
 t_h & S_1, S_0 \\
 & B, A \\
 & RIN, LIN \\
 & CLR \rightarrow Q \\
 & CLK \rightarrow Q \\
 & f_{MAX}
 \end{aligned}$$

- (c) By inspecting the results of Part (a), give the equations for D_A , D_B , D_C , D_D for a 4-bit version, that is for the 74LS194.

2. *Using* a 74LS194, design a sequence generator which cycles through the following sequence (top to bottom and back again):

0000
1000
1100
0110
1101
1011
0111
0011
0001

Have all unused states reset to 0000 (synchronously).

3. Repeat the above problem using a 74LS163 counter.