

ECE 561: Digital Circuit Design

Homework #6

Problems:

Use the VHDL editor in Xilinx to verify the correctness of your syntax for each of the following VHDL programs. Include the Xilinx printout of each VHDL program in your results.

1. Problem 6.47. Start with the VHDL program given in class for the 74x49. Redesign the VHDL seven-segment decoder according to the specifications in the problem (add tails for digits 6 and 9, and display the character “E” for nondecimal inputs 1010 through 1111). Also, change the seven-segment outputs so that they are all active low.
2. Write a VHDL program for the state machine of Problem 7.44. Use the state diagram given in the solution for Problem 7.44 in Homework #4.
3. Show how to modify Table 7-38 of the text to provide an asynchronous RESET input that forces the state machine to the INIT state. Repeat for a synchronous version that forces the state machine to the INIT state if RESET is asserted on the rising clock edge.
4. Problem 7-25.
 - (a) Use the StateCAD software in Xilinx (Tutorial: “Using Xilinx for State Machine Design”) to generate the VHDL program. Add a RESET signal to start the machine in state S0. Name the X input “XX” since “X” is not allowed as a signal name in StateCAD.
 - (b) Use the Xilinx simulator and verify that Z is generated correctly for the following sequence of inputs (after RESET):
X 0101100100
Y 0011101000

Include the state diagram and simulator trace from Xilinx in your results.