

ECE 561: Digital Circuit Design

Homework #8

Problem:

- This problem is much the same as the problem in the previous homework except that 15 persons, not just 2, are allowed in the room. You are to design the System Controller.

In this problem, P_1 and P_2 have been synchronized to the system clock (P_1'' and P_2'' generated) and a 74LS169 is employed to count the number of persons in the room. Recall that it is a 4-bit, up-down, binary synchronous counter and differs from the 74LS163 in two respects:

- The ENP , ENT , and RCO are all low-true asserted.
- The clear of the 74LS163 (CLR) has been replaced by an U/\bar{D} line which causes the counter to increment when "H" and decrement when "L". (No action occurs when the counter is not enabled.)

You are to design the System Controller:

- Give a block diagram for it,
- Provide a state diagram with a minimum number of states, and a state table, and
- Finish with a logic circuit diagram using NAND's, INVERTER's, and 74LS74 flip/flops.

Use the following architecture:

