The Ohio State University
Department of Electrical and Computer Engineering

ECE 561 **Digital Circuit Design** **Winter 2009**

Meeting Time:	8:30 am MWF, 120 Baker Systems
Instructor:	Professor David Orin
Office:	660 Dreese Lab
Office Hours:	after class MW
Grader:	Arjun Penumatsa (penumatsa.1@osu.edu)
Course Website:	http://www.ece.osu.edu/~orin/ece561
Textbook:	*Digital Design: Principles and Practices*, 4th Edition, by J. F. Wakerly
Textbook Website:	http://www.ddpp.com
Prerequisites:	ECE 206, 261, and prereq or concur 323
Computer Projects:	Using Xilinx on PCs running Windows XP
Xilinx Software Support:	Bea Jarupan, 600DL
	http://www.ece.osu.edu/xilinx
Grades Via Carmen:	http://carmen.osu.edu

Grading:	Quizzes	15%
(Tentative)	Computer Projects & Homeworks	25%
	Midterm Exam	30%
	Final Exam	30%

Course Topics

- Sequential circuit analysis (review).
- Timing issues (maximum clock frequency, setup time, hold time, clock skew).
- Sequential circuit design.
- Analysis of sequential circuits with logic building blocks and System Controller.
- System Controller design.
- More timing issues: asynchronous inputs, glitch-free outputs.
- Design with counters, shift registers, multiplexers, comparators, decoders, adders, PLDs, ROMs, and FPGAs.
- Design technology: VHDL, Xilinx.

Computer Projects

During the quarter, three or four computer projects will be assigned and graded. These projects will use the Xilinx software distributed with the book. The Department operates a PC lab with Xilinx software installed, and students may also use their own computers to execute designs. If you are going to use your own computer, be sure to download and install the latest software WebPACK from Xilinx. The projects are designed to reinforce concepts learned in class, to allow you to simulate and experiment with your designs, and to increase your exposure to CAD software and computers in general.

General Comments

1. There will be short quizzes (about ten minutes) on some Wednesdays. The lowest quiz grade will be dropped. As a result, there will be **no make-up quizzes**.

2. Homeworks will be assigned most weeks. They will typically be due on the following Wednesday in class. **No late homeworks** will be accepted. Solutions will be made available on the Carmen after the due date for the assignment.

3. One week's notice will be given to announce the day of each exam. Make-up exams will virtually NEVER be given.

4. Grading questions should be resolved within one week of the time when the graded work is returned. Check with the grader first and then with the instructor as needed.

5. Computer projects will be completed in groups of two, with one report turned in per group.

Class Schedule (Tentative)

Topic	# Periods	Text Reading
Sequential circuit analysis, timing	3	6.1*, 6.2, 7.1-2*, 7.3, 8.1, 8.2.1
Analysis of System Controller, counters, decoders, shift registers	5	6.4.1-4, 7.8 (pp. 587-8 only), 8.4.1-4, 8.5.1-5, 8.7
Sequential circuit design, developing state diagrams, finite-memory machines	3	7.4, 7.5
Design of 74x166 shift register, variable-entry maps, gating the clock, clock skew	2	8.8.1, 8.8.2
Review	1	
Midterm	1	
VHDL for decoder design, VHDL design of 74x49 seven-segment decoder	2	6.4.6
Flip-flops and state machines in VHDL	1	8.2.7, 7.12.1-4
Design of a binary serial adder, iterative circuits, adders	1	6.10.1-3, 8.6
Sequential circuit design using system controller, decomposing state machines, synchronous design methodology, 4-bit adder	3	7.8 (pp. 587-8 only), 8.7
Asynchronous inputs, output glitches	1	7.1.3, 8.4.4, 8.8.3
ROM-based design	1	9.1.1
PLDs	3	6.3.1-3, 8.3.1
FPGAs	2	9.6
Review	1	
Final	1	

* Review material.

Important reference pages:

SSI ICs	Figure 6-18, pg. 361
Timing for SSI parts	Table 6-2, pg. 366
Timing for MSI parts	Table 6-3, pg. 367
Timing for flip-flops	Table 8-1, pp. 684-5
SSI latch and flip-flop ICs	Figure 8-3, pg. 687
IC descriptions (page numbers)	Index, pg. 863