

ECE 662

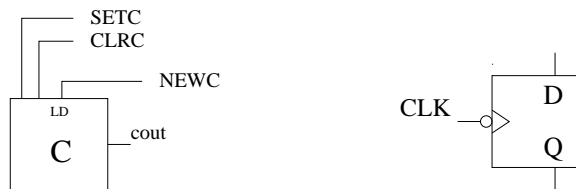
Homework #4

Problems:

In these problems, you will develop the circuitry for some of the elements of the datapath and control unit for the OSIAC 662.

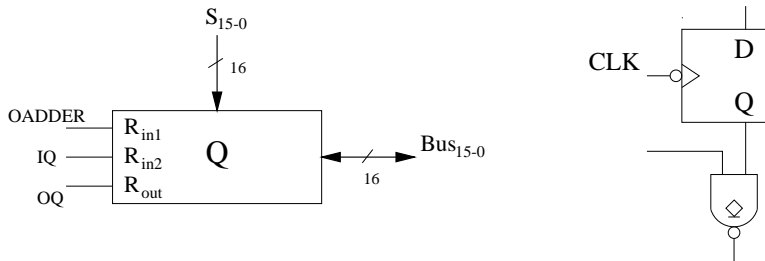
- Shown below on the left, is the block diagram for the 1-bit **C** condition code register. Note that it may be loaded with the new **cout** by asserting **NEWC**. It may also be set by asserting **SETC** and cleared by asserting **CLRC**.

Use the D flip-flop, shown on the right below, and a minimum number of NANDs and INVERTERS to design the 1-bit **C** register. Give the resulting logic circuit diagram. Assume that only one of **NEWC**, **SETC**, and **CLRC** may be asserted at a time.



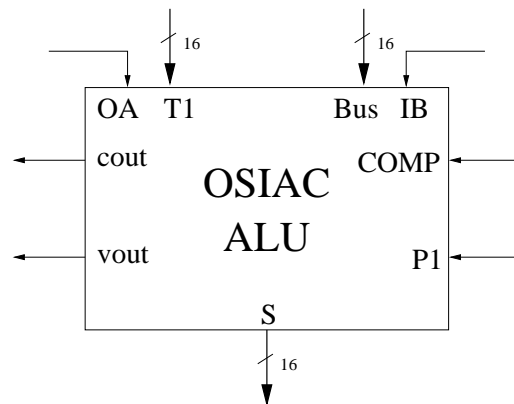
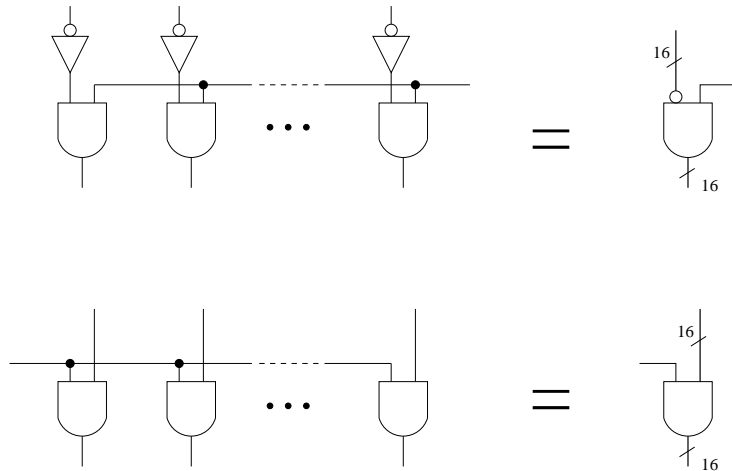
- Shown below on the left, is the block diagram for the 16-bit **Q** register. Note that it may be loaded with the output of the adder S_{15-0} by asserting **OADDER** and with the data on the **Bus** by asserting **IQ**. Its data may be furnished to the **Bus** by asserting **OQ**. Recall that the **Bus** is open-collector and low-true.

Use the circuit shown on the right below, and a minimum number of NANDs and INVERTERS to design the **Q** register. Assume that **IQ** and **OADDER** will not be asserted at the same time.



3. Shown at the bottom of the page is the block diagram for the 16-bit ALU. Note that T1 is furnished to the “A” side if OA is asserted. Otherwise, a 0 is input to the A side. Similarly, the Bus data is furnished to the “B” side if IB is asserted. Otherwise, a 0 is input to the B side. The basic unit of the ALU is an adder, and the B input may be complemented before entering it by asserting COMP. An additional 1 may be added by asserting P1.

Use the circuits show in the first two parts below (symbols on the right), and the “Binary Addition-Subtraction Logic Network” in Figure 6.3, pg. 371 of the text, as well as a minimum number of NANDs and INVERTERS to design the ALU. In Figure 6.3, break the connection between the Add/Sub control and c_0 before using the logic network. Give the resulting logic circuit diagram for the ALU. Note that Fig. 6.3 may be used in the solution, and all the carries inside the 16-bit adder may be assumed to be available.



4. Shown below is the block diagram for the combinational logic which selects the 4 general-purpose registers of the OSIAC 662. WAC determines whether Bus data will be written into one of the registers. The particular register number is determined by WN, IR₃₋₂ (src), or IR₁₋₀ (dst). RAC determines whether data from one of the registers will be read and placed on the Bus. The particular register number is determined by RN, IR₃₋₂ (src), or IR₁₋₀ (dst).

Use 4x1 MUXs and 2-to-4 decoders, and a minimum number of NORs and INVERTERS to design the combinational logic. The symbol for the MUX and decoder is given below. Give the resulting logic circuit diagram.

Hint: note that 2 MUXs with common S₁ and S₀ lines can multiplex 2-bit numbers.

