

The Ohio State University
Department of Electrical and Computer Engineering

ECE 662

Theory and Design of Digital Computers

Autumn 2007

Meeting Time: 2:30 pm MWF, 133 Caldwell Laboratory
Instructor: Professor David Orin, 660 Dreese Lab
Office Hours: 3:30 p.m. MW
Grader: Manasa Ramini, ramini.1@osu.edu, 601 Dreese Lab
Office Hours: 2-3:00 p.m. Thursday (for questions on grading)
Web Page: <http://ece.osu.edu/~orin/ece662>
Text: *Computer Organization*, 5th Ed., by C. Hamacher, Z. Vranesic, & S. Zaky
References: *Computer Architecture and Organization*, 3rd Ed, by John P. Hayes
Computer Architecture: A Quantitative Approach, 3rd Ed,
by J.L. Hennessy and D.A. Patterson
Prerequisites: ECE 265 or CSE 360, and ECE 561
Grades Via Carmen: <http://carmen.osu.edu>

Grading:	Homework	12%
(Tentative)	Machine Problems	18%
	Midterm Exam	30%
	Final Exam	40%

General Comments

1. One week's notice will be given to announce the day of the midterm exam. Make-up exams will virtually NEVER be given.
2. Homeworks will be assigned most weeks. They will typically be due on the following Wednesday in class. **No late homeworks** will be accepted. Solutions will be made available on the ECE 662 web site after the due date for the assignment.
3. Grading questions must be resolved within one week of the time when the graded work is returned. Check with the grader first and then with the instructor as needed.
4. Machine Problems include specifications for simple computers which are tested with a simulator program on the Unix workstations.

Class Schedule (Tentative)

Topic	Lecture	Reading
Basic structure of computers	1	1–18
Motorola 68000 reg. structure, Simple Computer example	2	130–132
Bus structures, counter design	3	Appendix A
Number formats, arithmetic operations, overflow	4	25–32, 368–371
Memory locations, addresses	5	33–37
Instructions & instruction sequencing	6	37–47
Addressing modes	7	48–58, 131–136
68000 instruction set	8	94–98, 136–144
		Appendix C
68000 stacks and subroutines	9	68–73, 146–151
ECE662 simulator	10	
OSIAC 662	11	411–425
OSIAC 662 – data paths	12	
OSIAC 662 – general-purpose registers, adder	13	
OSIAC 662 – open-collector bus, temporary regs.	14	
Hardwired control	15	425–429
Example Control Unit	16	
Encoder circuitry	17	
Review for midterm	18	
Midterm	19	
Microprogrammed control	20	429–435
Memory basics	21	291–295, 313–314
Cache memories	22	314–322
Cache example	23	
Cache mapping techniques	24	322–325
Machine problem	25	
Direct memory access	26	234–237
Bus arbitration	27	237–240
Fast adders	28	371–376
Multiplication	29	376–390
Review for final	30	