

Name: _____

Table number: _____

ECE 327: *Electronic Devices and Circuits Laboratory I*

Final Exam (580 points possible out of 200 points)

August 11, 2009

Description. *This exam tests your comprehension of the course material. The exam is cumulative. You are tested on applications from class and asked to show that you can apply what you learned to other applications. Additionally, you are given the opportunity to complete an additional lab project for extra points.*

*Treat this exam as an opportunity to connect with and extend the laboratory material. **Bonus points** have been sprinkled heavily throughout the test. You may complete **as much or as little** of the exam as you wish. **HOWEVER**, I encourage you to provide course feedback requested at the end of this exam.*

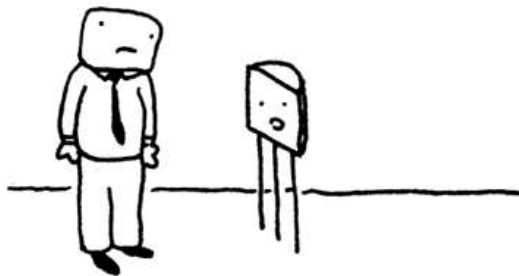
*Individual Work: This exam should be completed **individually**. Do not collaborate with your classmates nor consult any other person about the exam content. That is, **your answers should reflect your own work**.*

Resources: Feel free to use other published resources available to you (e.g., textbooks, on-line articles, supplementary class materials, etc.). Any of your own notes may be used as well.

After completing the exam, sign the honor pledge below if it applies. MAKE SURE YOU PUT YOUR NAME ON THE EXAM.

You may turn in the exam to my mailbox (i.e., "T. PAVLIC") in the ECE office (i.e., DL205). The secretary can date stamp it and make sure it gets into my mailbox. Alternatively, you may drop it off at my office (i.e., CL351). Please avoid sliding the exam under my office door unless absolutely necessary.

Date Due: Thursday, August 27, 2009 (**NOON** for graduating seniors and **11:59 PM** otherwise)



hi there! i'm a transistor! if it weren't for me, you'd have to go outside!

ECE honor pledge: "No aid given, received, or observed."

Signature: _____
(please sign if applicable)

Problem FE-1: Transistors and Impedance (55 points)

Consider the circuits in Figure FE-1.1. Assume that the transistor is in *active mode* (i.e., no *saturation* or *cutoff*).

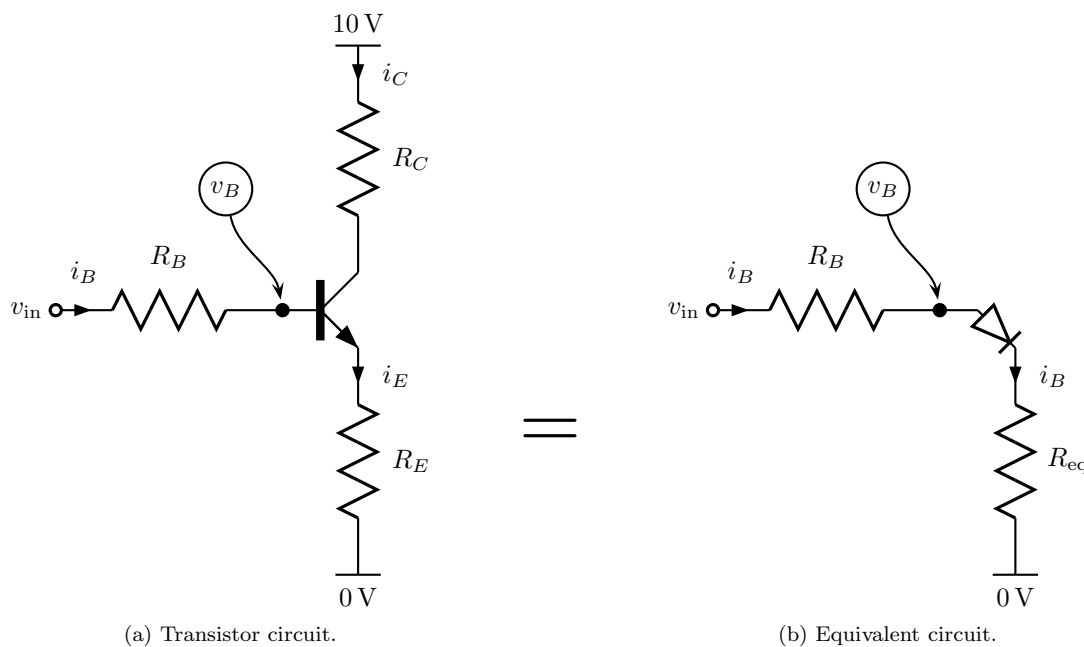


Figure FE-1.1: Transistor and equivalent circuit.

From the point of view of the input, the two circuits are identical. Assume that the transistor's base-emitter drop (and therefore the equivalent diode drop) is 0.7 V , $R_B > 0$, and $R_E > 0$. Also assume that the transistor has a current gain of $\beta < \infty$. The voltage (with respect to ground) at the *input* of the transistor is shown as v_B .

Practical Matters (25 points)

5. Assuming that β is very high, what is a good estimate of i_B ? **(5 points)**
6. Even when β is very high, an estimate of the base potential v_B is not trivial. Derive an expression for v_B in terms of v_{in} , R_B , R_E , β , and the base-emitter diode drop of 0.7 V. **(10 points)**
7. In the lab, we always make sure the Thévenin equivalent resistance looking *out of* the base of the transistor is very low compared to βR_E (where we assume that β has a low-end value of 100). Why? **(10 points)**

Problem FE-2: Voltage Regulator (80 points)

A Simpler Approach (45 points)

Consider the voltage regulator circuit in Figure FE-2.1.

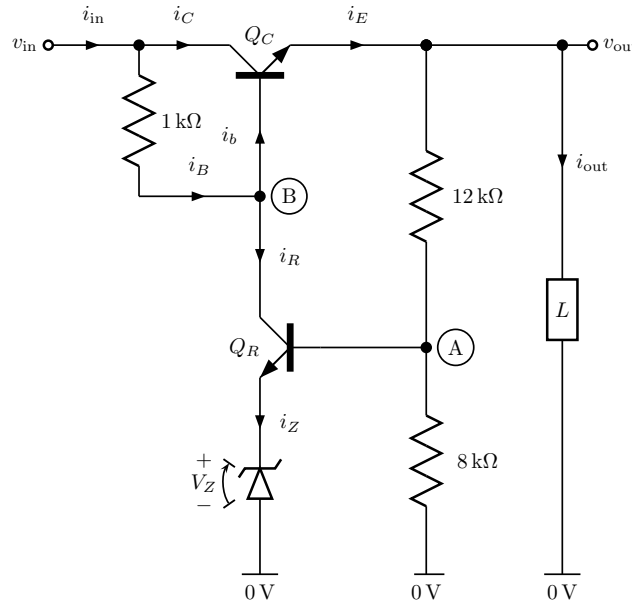


Figure FE-2.1: Voltage regulator with load L . Unless stated otherwise, $L = 10 \text{ k}\Omega$.

This circuit not only has considerably fewer components than the regulators we built in class, but it uses *different* components. Recall that a generic *forward* $i-v$ curve for a Zener diode is shaped like Figure FE-2.2.

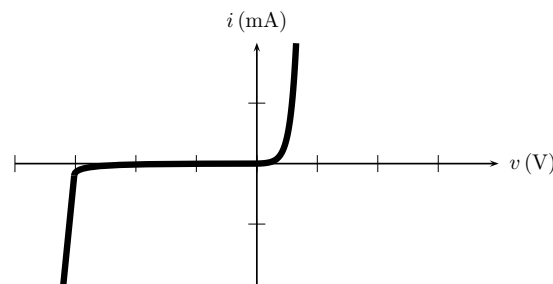


Figure FE-2.2: Generic (i.e., not to scale) Zener current-potential curve.

The Zener diode used in Figure FE-2.1 has *forward* current i that can be modeled by

$$i = \begin{cases} \frac{1}{28 \Omega} (v + 3.3 \text{ V}) - 0.020 \text{ A} & \text{if } v < -\frac{1096}{393} \text{ V} (\approx -2.79 \text{ V}) \\ \frac{1}{1600 \Omega} (v + 0.4 \text{ V}) - 0.00025 \text{ A} & \text{if } -\frac{1096}{393} \text{ V} (\approx -2.79 \text{ V}) \leq v < 0 \\ (0.2 \text{ A}) \left(\exp\left(\frac{550}{13}\right) - 1 \right)^{-1} \left(\exp\left(\frac{v}{0.026 \text{ V}}\right) - 1 \right) & \text{if } 0 \leq v, \end{cases} \quad (\text{FE-2.1})$$

where v is the diode's forward potential. Assume that

- (i) the v_{in} potential is provided by an ideal source.
- (ii) both transistors have current gain $\beta \gg 1$ (i.e., $\beta \approx \infty$).
- (iii) **the base-emitter drop of both Q_C and Q_R is 0.7 V .**

It is given that $v_{\text{out}} = 10 \text{ V}$.

1. For $v_{\text{out}} = 10\text{ V}$, what is the potential at node A? **(5 points)**

2. What current i_Z is necessary? **(5 points)**

3. What is the current i_R flowing through the Q_R transistor? **(5 points)**

4. What is the potential at node B? **(5 points)**

5. What is the current i_B flowing into node B? **(5 points)**

6. What is v_{in} ? **(5 points)**

7. How could the **LINE** regulation of this circuit be improved? **(10 points)**
*[HINT: Acceptable answers somehow involve [Figure FE-2.2](#) and [Equation \(FE-2.1\)](#). They describe the property of the element that controls the **line** regulation.]*

8. For $L = 10\text{ k}\Omega$, does Q_R or Q_C conduct more current? That is, is i_C or i_R higher? **(5 points)**

A Biased Approach (35 points)

For the following, consider the slightly different regulator in Figure FE-2.3. Note R_Z . Again, let $v_{out} = 10\text{ V}$.

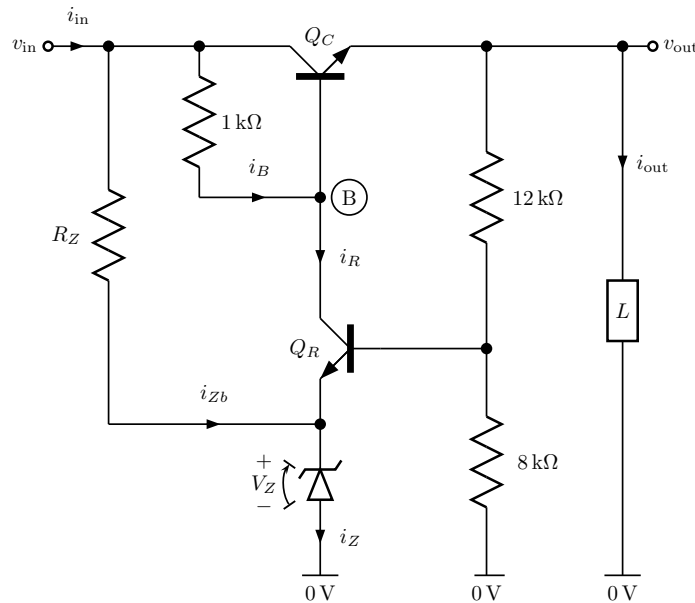


Figure FE-2.3: Modified voltage regulator with load L .

9. How does the new resistor R_Z allow us to change the i_R ? (5 points)

10. Does adding R_Z change the required v_{in} for $v_{out} = 10\text{ V}$? If so, how? If not, why? (10 points)

11. Ideally, in *both* regulators above, what happens to v_{out} as load L resistance greatly decreases? How does this result differ from the **ideal** discrete-transistor regulators used in class? (10 points)

12. How can the placement of R_Z be changed to improve the circuit's line regulation? (hint: is there a steadier voltage source in the schematic that can drive R_Z instead of v_{in} ?) (10 points)

Problem FE-3: Operational Amplifiers (40 points)

The Ideal Operational Amplifier (5 points)

The “block diagram” in [Figure FE-3.1](#) represents a generic *difference amplifier* with gain G .

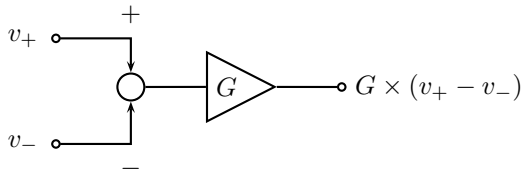


Figure FE-3.1: Generic difference amplifier.

1. An *ideal* operational amplifier is a difference amplifier with one special property. What is it? **(5 points)**

Practical Component Choice (5 points)

2. In nearly every lab, we were able to use the [LF351](#) operational amplifier. However, in the PWM demodulator lab, we had to use the [CA3160](#) even though it was a slightly slower operational amplifier. What is special about the [CA3160](#) operational amplifier that makes it ideal for sample-and-hold applications? **(5 points)**

Slew Rate and Integration (30 points)

Most operational amplifiers work by **diverting a fraction of a constant current** into or out of a **capacitor**. The greater the difference between its inputs, the greater the fraction. The operational amplifier's output is the voltage across the capacitor. In the following questions, **keep this *simplified* description in mind**.

3. Use this simplified description to explain how an operational amplifier *acts* like a *difference integrator*. **(15 points)**

4. Recall the relaxation oscillator that you built with an operational amplifier in the lab. The output of the oscillator appeared to be a square wave, but when you zoomed in on the rising and falling edges of the waveform, you saw that they were *slanted lines*. The slope of these lines was called the *slew rate* of the operational amplifier, and different operational amplifier models had different slew rates.

- (i) Assume that the input to the operational amplifier is a large *step* that immediately causes *all* of the *constant current* to be diverted into (or out of) the capacitor. Describe the output of the operational amplifier. **(10 points)**

- (ii) Assume that the constant current feeding the operational amplifier's input stage is I and the output capacitance is C . Derive the *slew rate* of the operational amplifier. (hints: What is the *maximum* capacitor current? What is its relationship to capacitor "speed"?) **(5 points)**

Side note: The capacitance used by the operational amplifier is strongly linked to its *bandwidth*. For high speed applications, operational amplifiers (like the CA3130) have no internal non-parasitic capacitors in their design — it is up to the user to add external capacitance (between the "compensation" pins) if necessary. This "compensation" is sometimes necessary to *stabilize* the resulting feedback system. Recall feedback topics from ECE 551/750 (e.g., root locus, lag compensation, phase margin, Nyquist plots, etc.).

Problem FE-4: Filters (75 points)

The following questions refer to the filter in Figure FE-4.1. Assume the output has no *clipping* distortion.

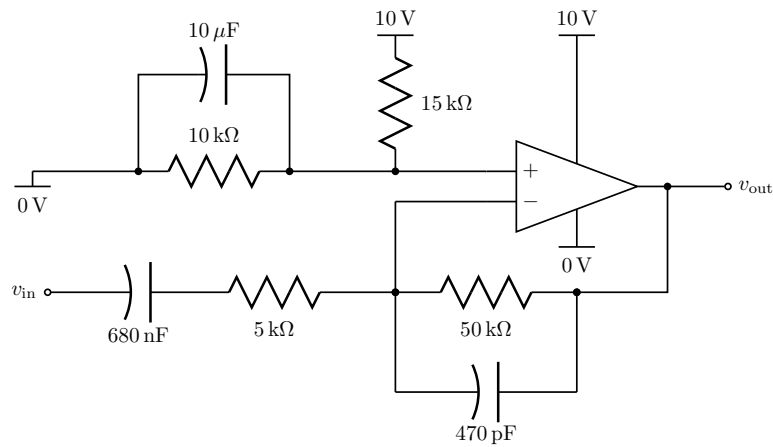


Figure FE-4.1: Operational amplifier filter

1. What is the ideal DC component of the output v_{out} ? **(5 points)**
2. What is the purpose of the $10\ \mu\text{F}$ capacitor? Why is it so much larger than the other capacitors? **(10 points)**
3. What is the ideal *passband gain* of the filter? Your answer should *NOT* be in terms of s . **(10 points)**

Problem FE-5: Relaxation Oscillators (150 points)

The following questions refer to the relaxation oscillator in Figure FE-5.1.

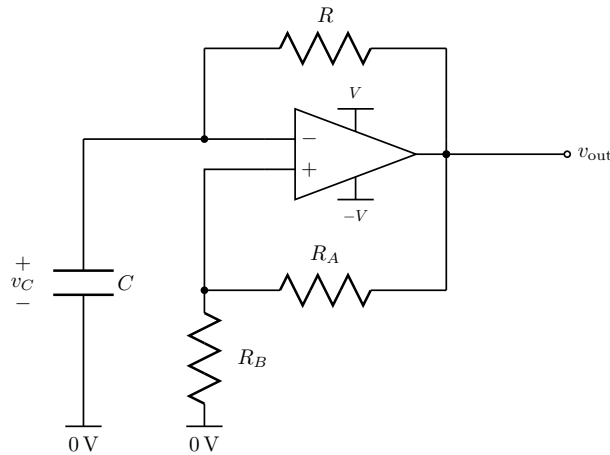


Figure FE-5.1: Operational amplifier relaxation oscillator: astable multivibrator.

Unless otherwise specified, assume that the operational amplifier (OA) can swing from **rail-to-rail** with **infinite slew rate**¹ and that $V > 0$, $R > 0$, $R_A > 0$, $R_B > 0$ and $C > 0$.

1. If we assume that $C > 0$ and the OA has **infinite** slew rate, the output v_{out} will be a square wave. More realistically, the OA will have **finite** slew rate and v_{out} will **not** be square. Draw each of the **two** possible non-square v_{out} shapes for a **finite** slew rate OA. **(10 points)**
2. In terms of the circuit parameters above, derive the **period** of the ideal v_{out} **square wave**. **(25 points)**
3. *Qualitatively* describe the impact on the circuit output if R_B is *increased*. **(10 points)**

¹Such an OA can be called a *comparator*.

4. *Qualitatively* describe the impact on the circuit output if R is *decreased*. **(10 points)**
5. If V is increased, does the **PERIOD** of the *output* of the circuit change? Why or why not? **(10 points)**
6. Assume that $V = 10\text{ V}$. Without adding any new components, how could you use this circuit to generate a square wave that periodically switches from -5 V to 5 V ? **(15 points)**
7. Assume that $V = 10\text{ V}$. Without adding any new components, how could you use this circuit to generate a periodic waveform that sweeps through *every* voltage between -5 V and 5 V ? **(20 points)**
8. If $C = 0$, then the capacitor can be replaced by an open circuit (i.e., the capacitor can be *removed*). **As usual**², assume that the OA has *finite* slew rate and has $v_{\text{out}}/(v_+ - v_-)$ transfer function $G/(s - p)$ where $G \gg 1$ and $p \leq 0$. What will v_{out} be in this $C = 0$ case? **(15 points)**

²We have (implicitly) made this assumption all quarter. For reasons why this model makes sense, see [Problem FE-3](#).

A Regular Old Modification (35 points)

This problem applies aspects of [Problem FE-2](#) to implementing real relaxation oscillators in the laboratory.

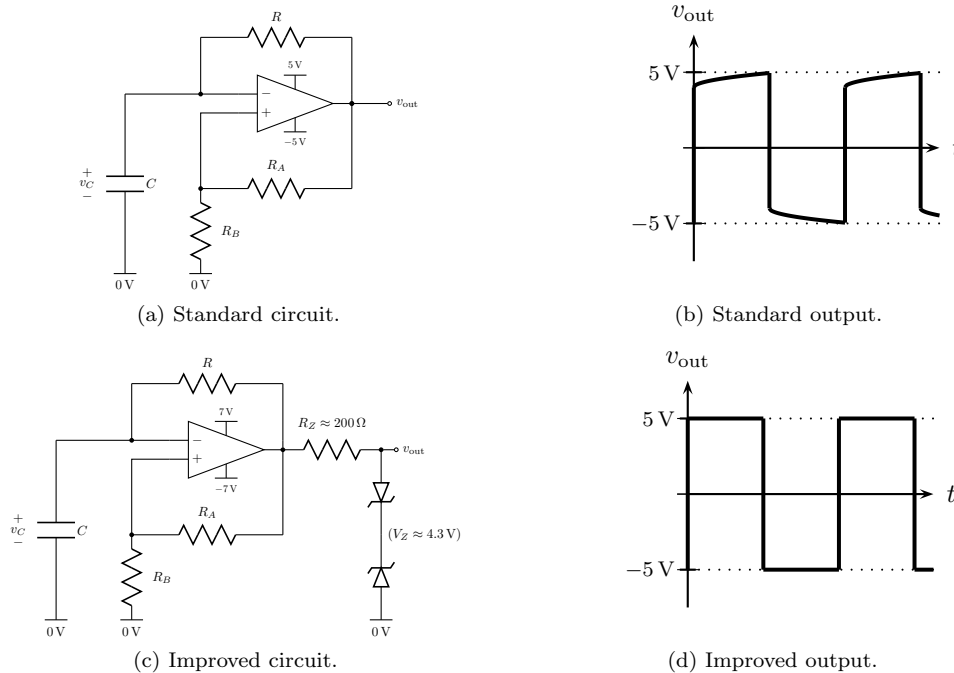


Figure FE-5.2: Relaxation oscillator variations.

You need to implement a square wave that oscillates from -5 V to 5 V . In the laboratory, you build [Figure FE-5.2\(a\)](#) using an [LM741](#) operational amplifier, and you see the output shown in [Figure FE-5.2\(b\)](#). Although this output has sufficiently vertical edges, the top and bottom of each pulse is curved and never quite reaches the desired 5 V amplitude.

A colleague suggests that you increase your supply rails from $\pm 5\text{ V}$ to $\pm 7\text{ V}$ and add a resistor and two Zener diodes on your circuit output. In particular, she tells you to use Zener diodes with nominal breakdown voltage of 4.3 V and to put them in series with each other as in [Figure FE-5.2\(c\)](#)³. You make the changes she suggests, and the result (at room temperature) is the desired output in [Figure FE-5.2\(d\)](#).

9. Explain why the old circuit fails and the new circuit works. (10 points)

³Matched Zener diodes connected in this way can be purchased as a single unit called a *double-anode Zener diode (DAZD)* or a *thyrector*. These units often are drawn as two opposing Zener diodes sharing a common “hat.”

10. Explain why the Zener diodes have opposite “polarity.” In particular, why isn’t a single Zener diode used? **(5 points)**
11. Your boss tells you that the designed power supply rails can be no larger than $\pm 5\text{ V}$, and so the new design is not acceptable. You e-mail your old ECE 327 TA, and he suggests you use the original design from [Figure FE-5.2\(a\)](#) with an operational amplifier (or even a comparator) with a CMOS output, like the [CA3160](#) operational amplifier. His suggestion also produces the desired output. Why? **(10 points)**

Your company has a surplus of [LM741](#) operational amplifiers, and so your boss wants you to use those parts for your project. You realize that your company also has a surplus of CMOS inverters, like the [CD4049](#). You implement the original circuit in [Figure FE-5.2\(a\)](#) with the original [LM741](#) part; however, you follow the circuit with a CMOS inverter with $\pm 5\text{ V}$ supply rails, and the “inverted” output looks perfect.

12. Explain why using the CMOS inverter solves the problem. **(5 points)**
13. If you fed back the output of the inverter (rather than the operational amplifier), how else would the circuit have to change? For simplicity, assume that the inverter is sufficiently fast. **(5 points)**

Problem FE-6: Current Sources as Inputs (25 points)

In typical undergraduate engineering classes, it is common to derive input-voltage–output-voltage transfer functions that represent the “gain” of a circuit at a particular frequency. However, input-current–output-voltage relationships can also be described by transfer functions; these $V_{\text{out}}/I_{\text{in}}$ transfer functions represent the “*transresistance*” (i.e., “**transfer resistance**”) or “*transimpedance*” at a particular frequency.

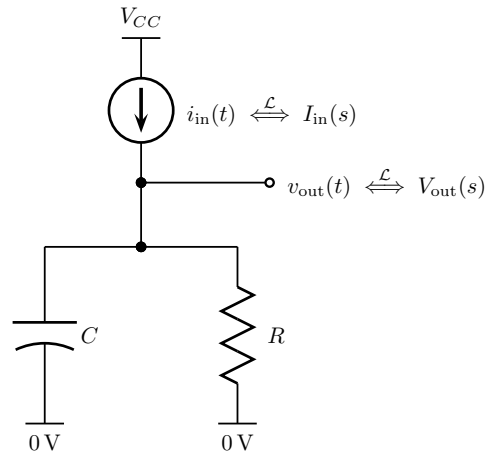


Figure FE-6.1: A current source driving a parallel RC load.

The following questions refer to [Figure FE-6.1](#). Assume that the current source is in *compliance* at all times.

1. What is the Laplace-domain $V_{\text{out}}(s)/I_{\text{in}}(s)$ transfer function (i.e., the “transimpedance”)? **(10 points)**

2. Explain how this circuit approximates an *integrator* when C , R , or both are very large. **(5 points)**

Ramp Generation from Step Responses (10 points)

The circuit in [Figure FE-6.1](#) models the **ramp generator** used in several of this quarter's laboratories. In particular, C is the chosen capacitor and R is a very large but **finite** *parasitic* resistance that originates from capacitor or switch leakage and/or breadboard imperfections.

3. Explain why ramp generators that used extremely small capacitors had *curved* ramps. **(5 points)**

4. In the laboratory ramp generators, why were *small* capacitors used? That is, why couldn't large capacitors be used instead? (**hint**: what else was connected across the capacitor?) **(5 points)**

Alternate Implementation and Practical Matters (100 points)

The circuit in [Figure FE-7.2\(a\)](#) also implements a current source.

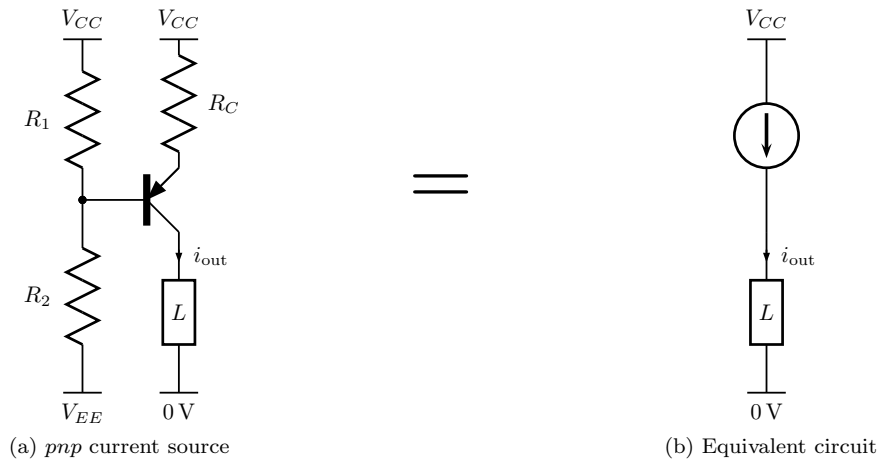


Figure FE-7.2: Alternate implementation of current source from [Figure FE-7.1](#).

3. Assume that $R_1 = R_2$, $V_{CC} = 12\text{ V}$, and $V_{EE} = 0\text{ V}$. Also assume that R_C and L are picked so that the current source is in compliance and the transistor is in active mode.

Because $R_1 = R_2$, you expect that the transistor's base voltage will be 6 V. However, after building the circuit you probe the base and it's 7 V.

- (i) What's wrong? Why does the voltage between R_1 and R_2 increase when the node is connected to the transistor base? **(10 points)**

- (ii) How do you fix the problem and still keep $R_1 = R_2$? **(5 points)**

- (iii) What's special about the diode biasing in [Figure FE-7.1\(a\)](#) that prevents this problem? **(10 points)**

4. When you probe the V_{CC} supply for the circuit in [Figure FE-7.2\(a\)](#), you notice relatively large ripples.
- (i) How do the power supply ripples affect i_{out} ? **(10 points)**

- (ii) Argue that the power supply ripples make it wrong to call this circuit a “common-base amplifier.” **(10 points)**

- (iii) How is the situation improved by using the diode biasing from [Figure FE-7.1\(a\)](#)? **(10 points)**

- (iv) You decide to use the diode biasing from [Figure FE-7.1\(a\)](#), but you still want to get rid of the supply ripples. So you add large power supply bypass capacitors throughout your circuit. However, because you have wired the two different V_{CC} connections to different spots on your breadboard, you now see more ripple on one V_{CC} than the other. Should you be concerned? Why or why not? **(10 points)**

5. In both Figure FE-7.1(a) and Figure FE-7.2(a), after applying power, the bipolar transistor becomes much warmer than the other elements of the circuit.

(i) What effect does the increased transistor temperature have on i_{out} ? Does it change? If so, how? **(10 points)**

(ii) How can the situation be improved by *physically mounting* one of the diodes to the transistor? **(10 points)**

(iii) Why is temperature compensation more effective when *integrating* components on the *same* piece of silicon (i.e., when doing an *integrated circuit (IC)* design)? **(10 points)**

(iv) The *output stage* of an amplifier usually has low voltage gain but can deliver *relatively* high current to the amplifier load. That is, these stages have *power gain*.

When designing or analyzing bipolar transistor output stages for high power applications, why is it common to assume that the base-emitter drop is *not* 0.7 V? Do you think a higher or lower value is used? **(5 points)**

Side note: Unipolar transistors (e.g., JFETs and MOSFETs) do not “runaway” like bipolar transistors. The “threshold voltage” for unipolar transistors decreases with temperature; however, the “gain” of the transistor also decreases with temperature. The combined effect is that hot transistors do not cook themselves; they’re thermally *stable*.

Problem FE-8: Current Sources as Loads (35 points)

Consider the *test fixture* in Figure FE-8.1. The *device under test (DUT)* is the (diode-biased) current source shown in Figure FE-7.1(a). The tester can set v_{test} to any voltage and measure I .

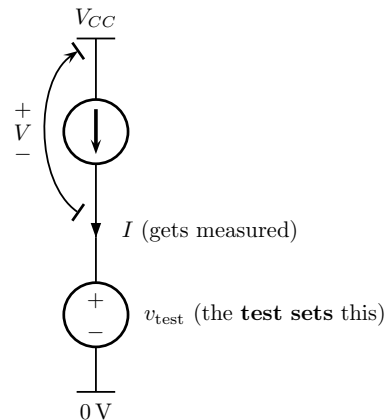


Figure FE-8.1: Current source test fixture. Current source is DUT.

Let

$$V \triangleq V_{CC} - v_{\text{test}}$$

be the voltage measured *across* the current source. The tester can set v_{test} and measure current I . Then the calculated V and measured I can be used to experimentally find the *impedance* of the current source. The *impedance* of a component represents how much the current through it changes when the voltage across it changes (e.g., roughly $\Delta V/\Delta I$).

1. Assuming that V is large enough for the current source to be in *compliance*, write a mathematical expression representing the I - V relationship of the current source. **(5 points)**

2. The impedance of a device is roughly defined by

$$\frac{\text{change in potential}}{\text{change in current}} = \frac{\Delta V}{\Delta I}$$

In other words, it's the *slope* of the I - V curve you just derived where I is on the horizontal axis and V is on the vertical axis. Assuming a current source is in compliance, what is its impedance? **(10 points)**

In Real Life (20 points)

HINTS: You should *read* the following paragraphs. Also, you should use what you learned in **this question above** to help you answer these questions.

If the collector of the transistor in Figure FE-1.1(a) was treated as an *output*, the resulting circuit would be a *common-emitter amplifier* with *emitter degeneration*. A pure common-emitter amplifier has $R_E = 0$. That is, it *fixes* the emitter potential so that changes in the base voltage cause changes in the collector voltage. There are several complications with setting $R_E = 0$, and so most modern common-emitter configurations assume $R_E > 0$. So it is usually implied that a *common-emitter amplifier* has a degenerated emitter. It is easy to verify that the small-signal (i.e., “AC”) gain of a common-emitter amplifier is roughly $-R_C/R_E$.

Sometimes an amplifier with *infinite gain* is needed. Because a transistor’s emitter always has some resistance, setting $R_E = 0$ does not give an infinite gain. Ideally, making R_C an *open circuit* would give an infinite gain, but the transistor cannot operate without having something connected to its collector.

3. When are (near-)infinite gain amplifiers useful? [*HINT: Op. amps are fodder for ...*] (5 points)

The CA3130 operational amplifier is shown in Figure FE-8.2.

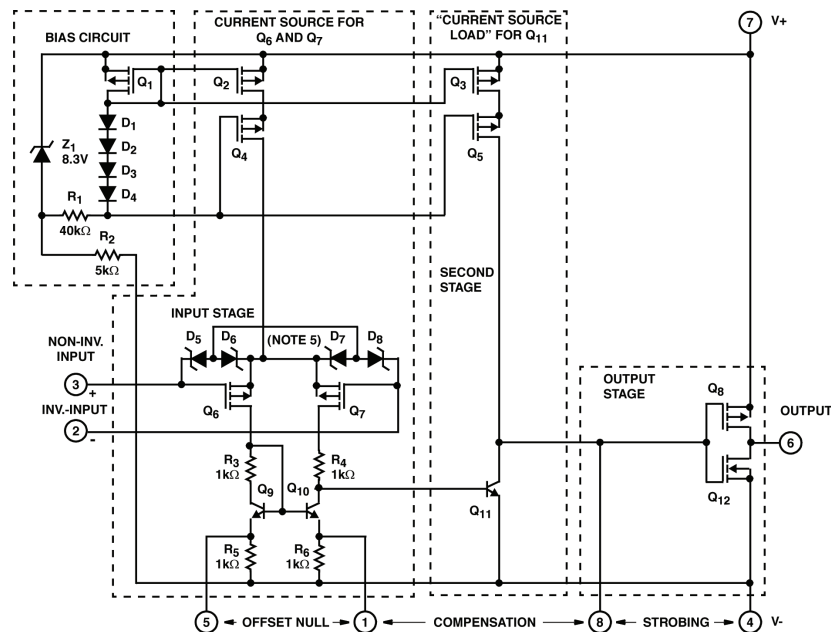


Figure FE-8.2: Schematic of CA3130 operational amplifier.

NOTE: Q_{11} is in a common-emitter configuration with $R_E = 0$. The Q_3 – Q_5 combination (called a “cascode,” which is spelled with an “o”) form a **current source** for the collector of Q_{11} (i.e., they *act* like load “ R_C ”).

4. Simply setting $R_E = 0$ does *not* give an infinite gain because of small intrinsic emitter resistance. However, the common-emitter amplifier setup by Q_{11} *does* have (near-)infinite gain. Why? (15 points)

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Optional: Course/Exam Feedback (10 bonus points)

By now, you should have been given several anonymous avenues for course feedback (e.g., via [Carmen](#), the registrar, and the SEI bubble sheets distributed in class). Your feedback is important to me so that I can improve my teaching styles and materials.

If you wish, please give me some feedback (positive OR NEGATIVE) about this final exam or about the course as a whole. You may leave this page attached to your final exam (i.e., non-anonymous feedback) or you may detach this page and return it to my ECE mailbox in the DL205 office. If your final exam is submitted with *ANY* feedback on this page **OR** if the page is detached, I will reward you **10 bonus points** on the exam.

Here are some **EXAMPLES** of questions that I have:

1. Were any parts of the **exam** unclear?
2. Is the **exam** too long/difficult/easy? Keep the bonus in mind.
3. Is the **exam** what you expected? (can you explain?)
4. Did the **exam** help to solidify what you learned in the class?
5. Did you learn anything while completing the **exam**?
6. Did the **exam** raise any additional questions about the course content?
7. Did the **exam** excite (or lessen!) your interest in the material at all?
8. Were the **quizzes** what you expected? Length? Difficulty? Helpful?
9. Did the **course** match your expectations?
10. What was your *most/least* favorite part of the **course**?
11. Do you feel there are topics not covered by the **course** that should have been? (can you explain?)
12. Was the **lab report grading** helpful? (can you explain?)
13. Do you have any **suggestions** or **ideas** about how any aspect of the **course** can be *improved*?
14. etc.

However, I welcome **ANY** feedback you have, even if it isn't related to anything in this list. Feel free to use the back of this page and/or additional sheets of paper (or e-mail me instead).