

# ECE 327: *Electronic Devices and Circuits Laboratory I*

## Lab 2: The Field Effect Transistor Quiz B (10 points)

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**Description.** This quiz tests your understanding of basic FET concepts. Here, we focus on the *n*-channel depletion-mode JFET and the *n*-channel and *p*-channel enhancement-mode MOSFETs. CMOS logic and switched-capacitor (SC) applications, like SC integrators, will also be explored. Be sure to read all instructions; there is a significant amount of bonus credit available on this quiz. Although you must complete this quiz with **closed notes**, you may use an **OPEN BOOK**.

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### Problem Q2-1: The JFET

1. What does JFET stand for? (1 point)

- **Junction Field Effect Transistor.**

The gate of a JFET forms a reverse-biased *pn*-junction (i.e., a reverse-biased diode) with the source and drain. For example, an *n*-channel JFET connects the source and drain with an *n*-type region and uses a *p*-type region for the gate. When operating properly, the gate potential must *not* be greater than either the source or the drain. The junction will be reverse-biased, and as the gate potential is decreased, a *depletion region* crowds out the *n*-channel and reduces current (i.e., increases resistance) through the device.

2. The conventional JFET is a *depletion-mode* device, which means that it is normally **on** (i.e., it is active when there is no potential difference between gate and source). (1 point)

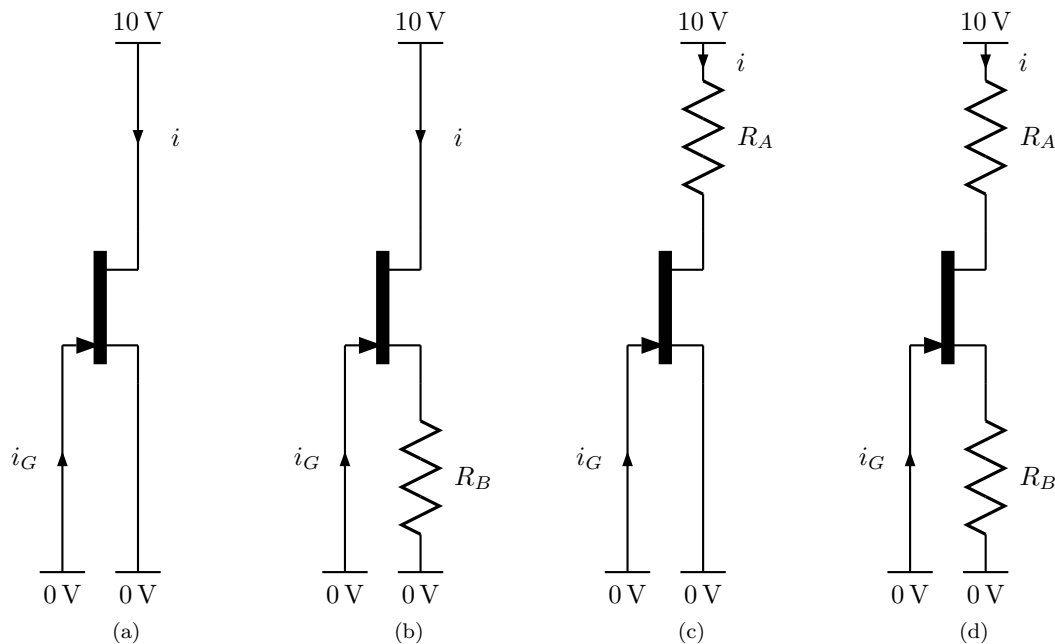
- When the gate and source of the JFET is shorted, the *pn*-junction sees a reverse bias from gate to drain, but it sees no bias from gate to source. Hence, the drain-side depletion region is large and the source-side depletion region is small. The resulting wedge-shaped channel acts like a constant (nonzero) current source (i.e., the current is turned *on*). Hence, the current is controlled by using the gate–source potential to increase the size of the *depletion region* in order to *decrease* the channel area. So the JFET is a *depletion-mode* device.

The following bonus questions refer to the four depletion-mode JFET circuits in [Figure Q2-1.1](#) on page 2. For each question, assume there is no gate leakage current (i.e., the ideal case), and also assume that  $R_A$  and  $R_B$  are chosen so that the JFETs are outside of their triode region (i.e., they are *active* in *pinch-off* mode).

3. Give the value of  $i_G$  for circuits (a) and (d). How do they compare? (2 bonus points)

- Ideally, both currents are equal to 0 A. The gate–source region of a JFET is reverse-biased, so no current will flow through the gate. In fact, there is no gate conduction in the conventional operation of any kind of FET. On the other hand, the base-emitter diode of a bipolar junction transistor must be forward biased, and so some small base current is unavoidable.

4. In (a), is the **gate potential** higher, lower, or the same as the **source potential**? (2 bonus points)
- The gate and source are both tied directly to 0 V, and so they both have the same potential.
5. In (b), is the **gate potential** higher, lower, or the same as the **source potential**? (2 bonus points)
- The positive current flowing through  $R_B$  raises the source potential *above* the gate potential. The result is that the gate potential is lower than the source potential.
6. In (d), which resistor(s) fixes the current  $i$ ? That is, is  $i$  determined by  $R_A$ ,  $R_B$ , or both? (2 bonus points)
- The current through a FET is determined by the gate–source potential. Therefore, *only*  $R_B$  affects the current. The resistor  $R_A$  may be viewed as a load. As long as  $R_A$  is not too large, the transistor will maintain a constant current through the load.
- Note that making  $R_A$  large will push the transistor out of its pinch-off (i.e., active) region and into its triode region (compare this to saturation of a bipolar junction transistor (BJT)). We assumed that we were not in the triode region, and so we implicitly assumed that  $R_A$  was sufficiently small.
7. Compare the current  $i$  in (c) and (d). Are they equal? If not, which one is higher? (2 bonus points)
- The maximum drain current through a depletion-mode JFET occurs when the gate–source potential difference is zero. Thus, the current  $i$  in (c) is higher than the current in (d).
- In (d), note that the gate potential is *lower* than the source potential. The gate–source junction is *always* reverse-biased in a depletion-mode JFET. So, for an  $n$ -channel depletion-mode JFET, the gate–source potential will *always* be non-positive.
8. Compare the current  $i$  in (a) and (c). Are they equal? If not, which one is higher? (2 bonus points)
- The current in a JFET is set by the gate–source potential only. These two circuits have the same gate potential and the same source potential, and so the currents are equal.

Figure Q2-1.1: Four depletion-mode  $n$ -channel JFET circuits.

## Problem Q2-2: The MOSFET

1. What does MOSFET stand for? (1 point)

- **Metal Oxide Semiconductor Field Effect Transistor.**

A *junction* FET (JFET) uses a reverse-biased diode (i.e., *pn-junction*) at its gate, and so its gate current is zero. Similarly, a MOSFET uses an oxide insulator (i.e., rust) between the gate and the rest of the transistor, and so it also has zero gate current. In both cases, the electric fields placed at the gate change the shape of the current-carrying channel connecting source and drain.

2. MOSFETs are also called IGFETs. What does IGFET stand for? The answer to this question is *not* in the laboratory text. (1 bonus point) **Insulated Gate Field Effect Transistor.**

See the previous answer for an explanation. Because most of the salient characteristics of FETs involve the method of gate insulation, the FET names often describe their gate types. Similarly, JFETs are often called JUGFETs (i.e., **J**unction **G**ate **F**ield **E**ffect **T**ransistor).

3. Compared to other transistors, the MOSFET has high gate (i.e., input) capacitance. In other words, the gate–source region acts like a capacitor. In fact, just it can be destroyed by too high of a voltage, just like a capacitor. What is a different problem associated with the high gate capacitance? (hint: a MOSFET will only respond to signals it can “see” across its gate–source region) (2 bonus points)

- MOSFETs have low bandwidth relative to other transistors (i.e., they are relatively “slow”). A result of the gate capacitance is that high frequency signals see a short circuit between gate and source. Therefore, these high frequency signals can be severely attenuated in the drain current.

JFETs do not suffer as greatly from this problem, and so they have higher bandwidth. Recall that JFETs achieve zero conduction by reverse-biasing a *pn*-junction at the gate, whereas MOSFETs insert an insulator between the gate at the rest of the transistor. The downside to the JFET configuration is that the gate must always be reverse-biased (e.g., the gate–source potential difference for an *n*-channel JFET can never be positive). Additionally, diode leakage is generally higher than capacitive leakage, and so JFETs have higher gate currents (though they still are much lower than BJT base currents).

Another FET that we do not discuss is the MESFET. The MESFET is very similar to the JFET, but it replaces the gate *pn*-junction with a Schottky junction (i.e., a metal-semiconductor junction). Non-traditional semiconductors are also used to make MESFETS (e.g., **GaAs** and **SiC**). These two characteristics give MESFETs extremely high bandwidth. They are common in high-frequency analog applications (e.g., microwave applications). They are less common in low-frequency applications because MESFET design is more difficult (i.e., more limiting) than other alternatives. That is, the existence of BJTs, JFETs, MOSFETs, and MESFETs reflects engineering tradeoffs.

In applications where the many advantages of FET design are needed along with some additional speed, FETs and BJTs are combined (e.g., the *BiFET*, *BiMOS*, and *BiCMOS* design methods).

- **NOTE:** As mentioned in the question, another related MOSFET downside is that the gate dielectric will breakdown when a large potential difference is placed across it. Permanent damage can be caused by even small static discharges from mishandling of devices with exposed MOSFETs.

The following bonus questions refer to the two circuits in [Figure Q2-2.1](#) on page 4. Note that the MOSFET symbols used here are different than the ones used in the laboratory text; however, the subcaptions below each subfigure indicate the meaning of the symbol. In particular, the circuit in (a) uses an *n*-channel enhancement-mode MOSFET, and the circuit in (b) uses a *p*-channel enhancement-mode MOSFET. For each of these questions, assume there is no gate leakage current (i.e., the ideal case), and also assume that the FETs are in their pinch-off (i.e., active) region. The operational amplifiers are ideal. (**hint:** recall the BJT common-emitter amplifier, and lean heavily on what you know about operational amplifiers)

4. In (a), what is the current  $i$ ? (4 bonus points)

- The operational amplifier adjusts the MOSFET's gate-source potential to keep the source potential at 4 V. That is, the 4 V at the noninverting (i.e., +) input of the OA is mirrored across the 2 k $\Omega$  resistor. Therefore, because the source and drain currents are the same, the drain current  $i$  through the 2 k $\Omega$  resistor is  $\boxed{2 \text{ mA}}$ .

5. In (a), what is the potential (i.e., "voltage") at node A (referenced to the 0 V nodes in the circuit)? (2 bonus points)

- Because the current  $i$  is 2 mA, the potential *drop* across the 8 k $\Omega$  resistor is 16 V. Therefore, the drain potential at node A is (30 V) - (16 V) =  $\boxed{14 \text{ V}}$ .

6. In (b), what is  $i_G$ ? (2 bonus points)

- With any FET, if there is no gate leakage current (i.e., the ideal case), the gate current will be  $\boxed{0 \text{ A}}$ .

7. In (b), what is the potential (i.e., "voltage") at node B (referenced to the 0 V node in the circuit)? (2 bonus points)

- The operational amplifier adjusts the MOSFET's gate-source potential to keep the source potential at (30 V) - (4 V) =  $\boxed{26 \text{ V}}$ . That is, the 4 V at the noninverting (i.e., +) input of the OA is mirrored across the 2 k $\Omega$  resistor.

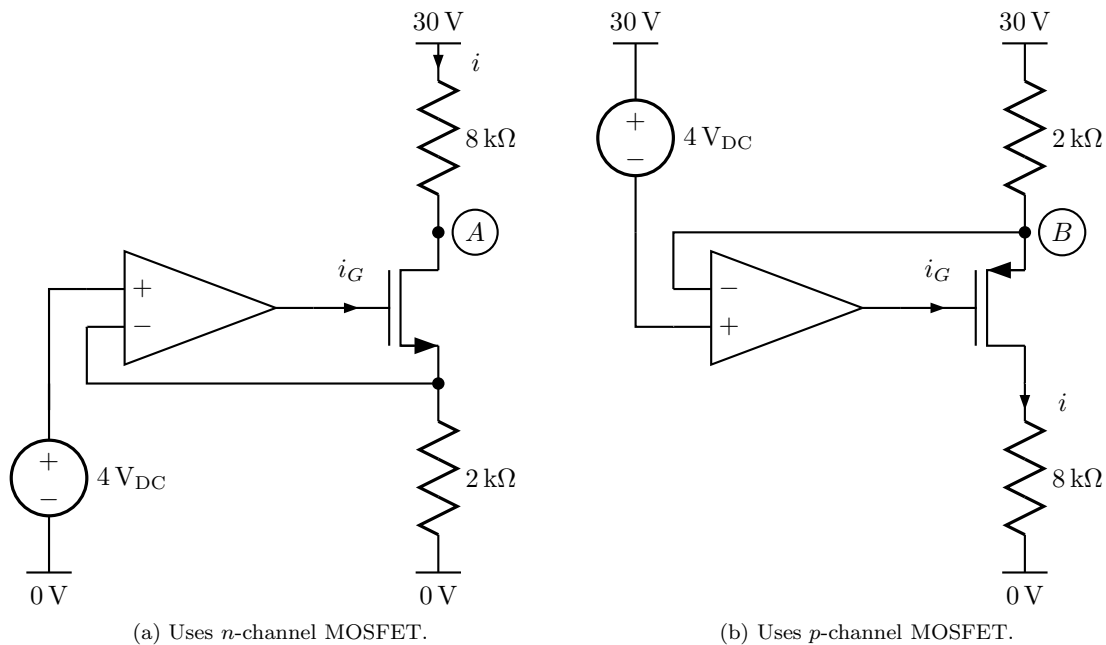


Figure Q2-2.1: Two enhancement-mode MOSFET circuits.

## Problem Q2-3: See You, CMOS

1. What does the **C** in CMOS stand for? (1 point)

- Complementary (or Complementary-symmetry).

A CMOS design couples  $n$ -channel MOSFETs with  $p$ -channel MOSFETs. Thus, CMOS design is a *complementary* MOSFET design method.

In particular, each CMOS design makes a symmetrical use of  $n$ -channel and  $p$ -channel MOSFETs. See the CMOS inverter and the CMOS linear switch in the lab manual for an example. Thus, some say that the **C** is not just for complementary but *complementary-symmetry*.

2. Ideally (i.e., assuming no leakage current), what is the current into the *input* of a (digital) CMOS inverter? (2 points)

- The input of a CMOS inverter feeds the gates of two MOSFETs, and so the input current will be

**0 A.**

Recall that the symbol for an inverter includes a triangle. This triangle is also used in the symbols for differential amplifiers (e.g., operational amplifiers), comparators, and buffers. The triangle symbol implies that the device has low input current (i.e., high input impedance) and (usually) low output impedance (or the contextual equivalent of high input impedance and low output impedance).

- **NOTE:** Because the input should be the high logic level or the low logic level (e.g.,  $V_{DD}$  or  $V_{SS}$ ) and nothing in between, one of the two MOSFETs in a CMOS inverter will always be in its subthreshold (i.e., “off”) mode. Hence, as long as the inverter’s output connects to a high impedance input (e.g., another CMOS gate input), the inverter supply current should also be nearly zero.

3. A  $p$ -channel enhancement-mode MOSFET can be made into a near perfect *switch*. When the negative supply voltage is present at the gate, holes from the two  $p$  regions are pulled toward the gate until a channel of very low resistance is formed (i.e., the switch “closes”). However, when the positive supply voltage is present at the gate, holes are forced away from the channel until it has extremely high resistance (i.e., the switch “opens”).

If a  $p$ -channel enhancement-mode MOSFET is being used as a switch and the switch is “closed”, then what happens as the signal “flowing” through the switch falls to very near the negative supply rail? (2 bonus points)

- When operated as a switch, the channel has very low resistance, and so the source and drain see the same potential (like any switch). So when the signal “in” the switch is pulled down to the same voltage as the gate, the source and drain both see the low gate voltage too. However, the channel will only be formed if holes are *more* attracted to the gate than they are to the source and drain. If the source and drain fall to the gate, the holes will stay in the source and drain, and the low-resistance channel will disappear. That is, the “closed” switch will “open.”

4. How do CMOS switches solve this problem? (3 bonus points)

- An  $n$ -channel enhancement-mode MOSFET switch is used “in parallel” with the  $p$ -channel enhancement-mode MOSFET switch, and a CMOS inverter is connected to the input of the  $n$ -channel switch. Now, the two switches open and close at the same time. Most importantly, whenever the low-resistance channel of one switch disappears, the low-resistance channel of the other switch will always be available. So a low-impedance current path is always present in this *complementary* configuration.

## Problem Q2-4: Switched-capacitor Integrators

Recall that *integrated circuits* are circuits with elements that share the same semiconductor (e.g., silicon) wafer. Elements are placed on the wafer by doping, etching, and depositing materials. So material properties of these elements can be matched very closely (e.g., transistors with the same gains and temperature characteristics; resistors with the same resistances; capacitors with the same capacitances; elements with properties that are precise ratios of other properties).

Conversely, the circuits that we build in our lab use *discrete elements*. For example, two resistors with the exact same color bands may have slightly different resistances. Of course, the chips we use are each examples of integrated circuits, but the circuits that we build with them are not.

1. Switched capacitors share many characteristics with resistors. In fact, provided a fast enough clock, they behave like resistors.

What is the main reason why switched capacitors (SC) are used instead of resistors *in integrated circuits*? (2 points)

- Capacitors and transistors use far less area than resistors. So using an SC as a resistor makes for a much smaller circuit footprint.

Additionally, SC resistances can be tuned by changing switching frequency. Tuning resistors on integrated circuits would otherwise require scrapping the original circuit and rebuilding a new one with a new physical resistor. For example, being able to tune resistances in the *field* has allowed for the production of integrated circuit *filters* whose frequency characteristics can be changed by the *user* rather than just the IC designer.

2. What switching frequency is required to emulate a  $5\text{ k}\Omega$  resistor with an SC that uses a  $10\text{ nF}$  capacitor? (2 points)

- Use the formula

$$R_{\text{eq}} = \frac{1}{f_{\text{clock}}C}$$

where  $R_{\text{eq}}$  is the equivalent resistance (i.e.,  $R_{\text{eq}} = 5\text{ k}\Omega$ ),  $f_{\text{clock}}$  is the clock frequency, and  $C$  is the capacitor's capacitance (i.e.,  $C = 10\text{ nF}$ ).

So

$$f_{\text{clock}} = \frac{1}{R_{\text{eq}}C} = \frac{1}{(5\text{ k}\Omega)(10\text{ nF})} = \frac{1}{50\text{ }\mu\text{s}} = 0.02\text{ MHz} = 20\text{ kHz}.$$

Therefore, the desired switching frequency is 20 kHz.

3. The operational-amplifier-based integrators you will build in this laboratory take square waves that *must* have exactly zero average value in order for the integrators to work.

Why do the inputs need *exactly* zero average/DC value? (5 bonus points)

- An operational amplifier is used to produce the output of the integrator. If the potential difference across the feedback capacitor grows to the size of one of the OA's rails, the capacitor will not be able to pump more charge into the capacitor and the output will be clipped (i.e., flat instead of sloped).

Square waves with no DC component are positive for a short time and then negative in exactly the same amount for exactly the same amount of time. As long as the period of the square wave is not too large, the capacitor will never have enough time to gather a potential difference too large for the operational amplifier. The result will be a triangular wave, which is the integral of a square wave.

If the square wave does not have a zero average (e.g., it's shifted or its duty cycle is different than 50%), over time the capacitor will accumulate a potential difference across it and the operational amplifier will clip the triangular output at its rails.