

Anisha Ramesh

Education

2006-present *Ohio State University*

Phd. Candidate Electrical Engineering

Working in Solid State Electronics & Photonics group under Prof. Paul R. Berger

- GPA – 4.0/4.0

2004-2006 *Indian Institute of Technology, Bombay, India*

MS. Electrical Engineering (Microelectronics)

- GPA – 9.6/10

Thesis Title - "Investigation of $\text{Bi}_{0.6}\text{Dy}_{0.3}\text{La}_{0.1}\text{FeO}_3$ Multiferroic Thin Films for possible use as a Memory Element"

2003-2004 *Centre for Development of Advanced Computing (C-DAC) Hyderabad, India*

Diploma in VLSI Design

- % of marks - 88.56

Project Title - "Design and Implementation of a Real-Time kernel on an FPGA"

1998-2002 *College of Engineering and Technology, Bhubaneswar, India*

BTech. Instrumentation and Electronics Engineering

- GPA – 8.74/10

Thesis Title - "Voice Controlled switch operation using speech recognition"

Achievements/ Awards

- Recipient of OSU University Fellowship 2006-07
- Awarded Best Student in Diploma in VLSI design by C-DAC, Hyderabad.
- 2nd in university (batch of 150 students) in graduation
- Recipient of All-India level NCERT scholarship (NTSE scholar)

Paper Publications

- Ronghua Yu, **R. Anisha**, Niu Jin, Sung-Yong Chung, Paul R. Berger, Thomas J. Gramila, and Phillip E. Thompson, "Observation of strain in pseudomorphic $\text{Si}_{1-x}\text{Ge}_x$ by tracking phonon participation in Si/SiGe resonant interband tunnel diodes via electron tunneling spectroscopy", *J. of App. Phys.*, 106, 034501, Aug 2009
- P.E. Thompson, G.G. Jernigan, S.-Y. Park, R. Yu, **R. Anisha**, P.R. Berger, D. Pawlik, R. Krom and S.L. Rommel, "P and B doped Si resonant interband tunnel diodes with as-grown negative differential resistance", *Elec.. Lett.*, 45(14), 759, July 2009

- **R. Anisha**, Niu Jin, Sung-Yong Chung, Ronghua Yu, Paul R. Berger, and Phillip E. Thompson, "Strain Engineered Si/SiGe Resonant Interband Tunneling Diodes with Outside Barriers Grown on Si_{0.8}Ge_{0.2} Virtual Substrates", *Appl. Phys. Lett.*, 93, 102113, Sept. 2008
- V.R. Palkar, **R. Anisha**, R. Pinto and S. Bhattacharya, "Multiferroic Behavior of Dy Modified BiFeO₃ Thin Films in Comparison with Tb modified BiFeO₃ Thin films ", *J. Mater. Res.*, 22(8), 2068, Aug 2007

Conference Presentations

- Si-Young Park, **R. Anisha**, Paul R. Berger, Roger Loo, Ngoc Duy Nguyen, Shotaro Takeuchi and Matty Caymax, "200 nm Si/SiGe Resonant Interband Tunnel Diodes Incorporating δ doping layers grown by CVD", *6th International Conf. on Silicon Epitaxy and Heterostructure (ICSI-6)*, May 17-21, 2009
- Phillip E. Thompson, Glenn G. Jernigan, Si-Young Park, Ronghua Yu, **R. Anisha**, Paul R. Berger, David Pawlik, Raymond Krom, and Sean L. Rommel, "Simplified Si Resonant Interband Tunnel Diodes", *presented at the International Semiconductor Device Research Symposium (ISDRS)*, Dec. 12-14, 2007.
- R. Krom, D. J. Pawlik, S. Muhkerjee, S. Pandharpure, S. K. Kurinec, S-Y. Park, R. Yu, **R. Anisha**, P. R. Berger, P. E. Thompson, and S. L. Rommel, "Anneal Time Study of Si Resonant Interband Tunnel Diodes Grown by Low-Temperature Molecular-Beam Epitaxy", *presented at the International Semiconductor Device Research Symposium (ISDRS)*, Dec. 12-14, 2007.
- D. J. Pawlik, S. Muhkerjee, R. Krom, S. Pandharpure, S. K. Kurinec, **R. Anisha**, P. R. Berger, and S. L. Rommel, "Temperature Dependent Empirical Modeling of Proximity Diffused Si Esaki Diodes and Memory Circuits", *presented at the International Semiconductor Device Research Symposium (ISDRS)*, Dec. 12-14, 2007.
- V.R. Palkar, **A. Ramesh**, R. Pinto and S. Bhattacharya, "Multiferroic Behavior of Modified BiFeO₃ Thin Films at Room Temperature", *presented at Ferroelectrics UK 2006*, May 23-25, 2006
- Vaijayanti Raghunath Palkar, **Anisha Ramesh**, Shashank Purandre, Smita Gohil, Richard Pinto and Shobo Bhattacharya, "Novel Multiferroic Thin Films of Modified BiFeO₃ for Non-Volatile Memory Applications", *presented at 2006 MRS Spring Meeting*, San Francisco, California, April 17-21, 2006
- **R. Anisha**, V.R. Palkar, J. John, S. Gohil, S.C. Purandre, R. Pinto and S. Bhattacharya, "Growth of Single Phase Multiferroic Bi_{0.6}Dy_{0.3}La_{0.1}FeO₃ using Pulsed Laser Deposition", *poster presented at International Conference of Optoelectronic Materials and Thin Films for Advanced Technology (OMTAT-2005)*, October 24-27, 2005

Work Experience

Sept 2008-Feb. 2009 Interuniversity Microelectronics Center (IMEC), Leuven, Belgium

International Scholar

- III-V passivation using anodic oxidation

Sept 2003- July 2004 Centre for Development of Advanced Computing Hyderabad,

India

Technical Member

- Involved in development of a research and development project entitled “Design and Development of a Transparent Solution for Securing Networks and Systems”, funded by Department of Information and Technology, Government of India. The project involved adding certain features to the Linux kernel for enhanced network security.
- Delivered lectures on Cryptography and Network Security Protocols in workshops conducted as part of the project, aimed at creating network security awareness in banks and defense organizations in India.
- Faculty Member for Diploma in Embedded Systems program.

Teaching Experience

Spring 2009 Ohio State University

Teaching Assistant for **ECE 327**, Electrical Circuits

Class size of 24 consisting of ECE Undergraduate students

Spring 2008 Ohio State University

Teaching Assistant for **ECE 300**, Electrical Circuits

Class size of 220 consisting of non-ECE Undergraduate students

Winter 2008 Ohio State University

Teaching Assistant for **ECE 300**, Electrical Circuits

Class size of 240 consisting of non-ECE Undergraduate students

Fall 2007 Ohio State University

Teaching Assistant for **ECE 637**, Solid State Microelectronics Laboratory

Class size of 16 consisting of ECE Graduate and Senior Undergraduate students

2004-2006 Indian Institute of Technology, Bombay, India

Teaching Assistant for **EE219**, Electronics Lab

Handled a group of 6 students (in a class of 50) consisting of ECE sophomores

2003-2004 Centre for Development of Advanced Computing, Hyderabad, India

Member of faculty, taught Intel 386 architecture and programming, Real Time Operating Systems and C Programming Lab

Class of 60, all ECE graduate students

Simulation Tools

- Cadence Design Kit
 - Virtuoso Spectre Circuit Simulator
 - Virtuoso Schematic Composer
 - Virtuoso Layout Editor
- Calibre DRC, LVS, xRC tools
- Agilent ADS (Advanced Design System)
- Silvaco VWF (Virtual Wafer Fab) Tools
- HDL Simulation – ModelSim

- HDL Synthesis - Leonardo Spectrum
- Verilog
- VHDL
- Veriloga

- C
- C++