CHAPTER 1

INTRODUCTION

Low power microelectronics has advanced in productivity and performance with an enormous pace, since the invention of transistor in 1947. The requirement for small size and weight, long operating life, utility, and reliability of battery operated equipment was the earliest demand for low power microelectronics. Personal Digital Assistant (PDA), which is characterized as a combined pocket cellular phone, pager, e-mail terminal, fax, computer, calendar, address directory, notebook, etc. had an explosive growth [1, 2], and many approaches were proposed to satisfy the needs of the Personal Digital Assistant for low power electronics [3-7].

After the new micro-power techniques of the 1970s and shifting from NMOS and NPN bipolar technologies to CMOS technology in order to solve the heat removal problems, 1990s brought low power design to the forefront as a primary requirement for mainstream microelectronics [8]. The future opportunities for low power giga-scale integration started to be discussed.

The power supply voltage in VLSI circuits, on the other hand, has decreased to 3V and will continue to decrease. The three main driving forces for low voltage low power systems are technology, design and market. Technology-driven forces come from the reduction of the minimum feature size to scale down the chip area. Scaling down the transistor size can then integrate more circuit components in a single chip area and lower the cost. Also, smaller geometry usually lowers the parasitic capacitances, which means higher operating speed and lower power consumption. A decrease in MOS transistor size means reduced gate oxide thickness as well as reduced channel length. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced.

With the reduction of the device minimum feature size, millions of transistors can be fabricated on the same chip. This will result in a tremendous power consumption and cause excessive heating. Usually most of the chip area is occupied by the digital circuits and the average power consumption for digital circuits is proportional to the square of the power supply voltage. Thus, decrease of the supply voltage reduces the power consumption in a significant amount.

All the above factors contribute to the necessity of low voltage low power circuit solutions. Since digital circuits occupy most of the chip area; they are more popular and computer-aided design tools for digital circuits are very mature. Digital circuit performances do not suffer a lot from lowering supply voltages. On the other hand, analog circuit performances are strongly affected by the low voltage supply. Therefore, new design techniques for low voltage analog circuits are required to be developed. In digital circuit design, a low supply voltage almost guarantees the low power consumption. However, this is not always the case for analog circuit design. To achieve the same goal of circuit performances by either using a low or a higher supply voltage might lead to approximately the same level of power consumption because of the different circuit design techniques utilized for using different supply voltages. Thus, low voltage analog circuit design with the emphasis of low power consumption has become a major challenge for analog circuit designers [9].

The development of analog circuits requires both a complete understanding of basic circuit design techniques and a knowledge of transistor nonideality effects on circuit performance. One severe effect comes from the device imperfections and variances of the fabrication process. Despite the technological progress in the fabrication process steps, the fluctuation in each step that affects the device performances have not been scaled down in proportion. The fabrication process is not easily characterized because these variations are random in nature. Such variations could ultimately be a limiting factor on how low the supply voltage and how reliable sub-micron designs could be. In order to produce manufacturable analog integrated circuits with high functional yield and a high degree of reliability, the design of such circuits must be robust with respect to random process and device parameter variations [10]. The functional yield of a chip is the percentage of the total number of circuit samples which have an acceptable circuit performance determined by the chip specifications, over the total number of circuit samples. This is different from catastrophic or destructive yield over which circuit designers have no control. Circuit designers must ensure that their chips have an acceptable functional yield under all manufacturing process variations. If there is more than one sample of the circuit on the same chip, the number of working circuits might be high, but in order to have a high functional yield the number of the circuits working with the required performance should be as high as possible. There are two ways to increase the functional yield: By improving the control of manufacturing process and by designing the process and circuits in such a way as to minimize the effect of inherent variations of the process on performance. The latter is typically referred to as “statistical design”. The statistical design problem is clearly to find a set of nominal component values and their tolerances that represent the minimum on the cost versus yield curve shown in Figure 1.1.

Due to inherent fluctuations in any integrated circuit manufacturing process, the functional yield is always less than 100%. As the complexity of VLSI chips increase, and the dimensions of VLSI devices decrease, the sensitivity of performance to process fluctuations increases, thus further reducing the functional yield. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed-signal chip.

Many meaningful insights have been provided into the statistical design problem. Early works have suffered from having only a few variables [11, 12] or simply consuming excessive CPU time [13]. An efficient technique was presented for yield gradient computation [14]; the number of design variables was primarily limited by the selected constrained nonlinear optimization algorithm in this work. Shyu et al. [15, 16] used statistical methods to examine the random errors affecting capacitance and current ratios

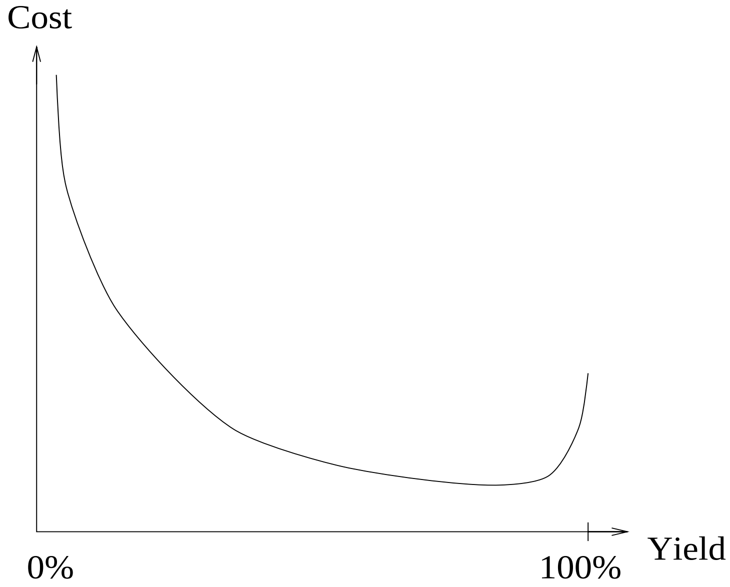

Figure 1.1: A typical circuit cost versus yield curve

in MOS integrated circuits. Explicit formulas were derived to give the dependence of each error source on the physical dimensions, the standard deviations of the fabrication parameters, the bias conditions, etc. All transistor variances were derived in terms of their effect on current matching in a current mirror. Additionally, Shyu examined edge effects which explain the variance of channel length and width. Lakshmikumar et al. [17] furthered Shyu's work and separated the area dependence of transistor mismatch into variance models for the threshold, V_T, and the current factor, β. Pelgrom et al. [18] included a term for the substrate factor variance and also altered the effect of global variations from a constant. Pelgrom also determined that edge effects have a negligible contribution to the overall variance of the current factor. However, it is expected that for very short or narrow devices, edge effects will contribute heavily to the parameter variance. Michael et al. [19] included the correlations among electrical parameters which were not included in Pelgrom's model. The statistical MOS (SMOS) model was presented as a tool for circuit designers to estimate the functional yield of a designed circuit without the fabrication of the device [19]. With the increasing popularity of BiCMOS technology, statistical methods are becoming necessary for BJTs too. The work of Michael has been extended to BiCMOS circuits and an appropriate test structure for BJT parameter mismatch extraction and characterization has been discussed in [20]. Abel at al. [21] showed that the current mismatch of a pair of MOS transistors at any bias point can be represented by mismatches in four standard MOS parameters: V_{TO}, γ, β and θ. The mismatch of a standard MOS parameter, $\sigma(\Delta P)$, in a large sample of matched transistor pairs is inversely proportional to the square root of the areas of the individual transistors. A graphical approach for the statistical design of RF circuits and systems was given in [22]. Recently, a new test structure for the characterization of MOS transistor mismatch and mismatch drift was presented [23]. Another recent work investigates MOS transistor mismatch and presents a methodology for optimizing mismatch without increasing layout area [24]. The work also examines edge effects and proves that the channel length and width reduction terms have very significant contributions to the area when considered for mismatch. In reference [25], the device matching issues of submicron analog CMOS circuits are addressed.

This study demonstrates the critical need to perform statistical design and optimization in order to enhance both the functional yield and reliability of low voltage low power analog VLSI circuits. The term “enhancing functional yield” stands for using tools and techniques that will target a high functional yield, by reducing the standard deviation of the circuit performance, instead of the typical methods of designing and hoping for the best yield. If the circuits are not optimized the variation of the performance may be very large, thus, the distribution will also be high. After optimization, however, it is possible to reduce the variation and keep the distribution smaller, thus, the yield will be higher. In industry, usually the yield requirement is initially set (e.g., to 99%) and the statistical modeling and statistical design of the circuits target this yield specification. The term statistical design includes the whole process of trying to make a robust design. The success of the chip is determined by how high the yield is; a high yield also reduces the cost. In this thesis, the yield specification is not initially set. It is the goal to show that it is possible to enhance the yield by reducing the standard deviation of the performance and optimizing the circuit.

Previous studies in the area of statistical modeling and simulations were separately successful in determining both the functionality of parameter mismatch variance and a methodology to simulate circuits. Merging the results of these two fields into a unified method to model and simulate performance variances in circuits containing MOS devices has resulted in the well known SMOS model which accounts for parameter correlations and physical layout information (e.g., device area and on-chip separation distance) [10].

The robust design process, in this thesis is the usage of the statistical MOS (SMOS) model to include the random process variations into the simulation environment, and the statistical techniques, such as Design of Experiments (DOE) and Response Surface Methodology (RSM), to determine the most important transistors for the circuit performance, and the optimum size for these transistors. The final objective, besides keeping the functional yield high, is to give flexibility to the designer, in finding the optimum size for the transistors. The response surfaces will provide this flexibility. The complete statistical design methodology is explained in Chapter 2. It is noteworthy that using statistical techniques such as DOE and RSM, together with the SMOS model, to make robust analog CMOS circuit designs is the first serious attempt with this thesis.

Chapter 3 describes the circuits that will be later statistically examined in Chapter 4. The circuits are selected among those which are subject to attention recently. The transconductor and multiplier circuits, however, are new designs for the thesis. The strategy behind these new designs are emphasized in the next page. All circuits are not the only examples of their types, and not the only circuits used for their purpose, but they certainly are one of the most popular, and recently used in several areas. These circuits are two low voltage and low power CMOS square-law analog composite cells, two transconductors and multipliers which use the low voltage and low power composite cells as a main building block, the four-MOSFET structure, and the 10-bit current division network, which are critical blocks in determining the overall performance of the designs they are used in.

Many applications which require reduced supply voltage and low power consumption are based on analog/digital mixed mode signal processing VLSIs. To process analog signals in such mixed mode systems, low voltage low power transconductors and/or multipliers have been widely used for programmability. These circuits are basicly composed of several cells which have a square-law characteristic. A single MOSFET fulfills this characteristic, however, the low input impedance at the source of the transistor limits the applicability of the single transistor solution. Recently, several new low voltage low power CMOS square-law composite cells with two high impedance input terminals were proposed to achieve highly accurate signal processing with low power dissipation. The design and operation principles of two of these cells are introduced in Chapter 3. Two new low voltage low power transconductors and multipliers were designed with these cells. The circuit description of the transconductors and multipliers are also given in Chapter 3. The first transconductor and multiplier circuits operate from a low supply voltage and maintains a wide input voltage swing capability. The second transconductor and multiplier circuits have the advantage of a low standby current, therefore, the circuits are more attractive for low power applications.

One discussion is made for analog circuits being programmable as in the digital area. The long range goals are to make analog circuits programmable, and to realize applications involving analog computation. The goal is to come up with an analog design methodology similar to the one used for digital circuits, and take advantage of the basic building blocks. The low voltage and low power cells of this thesis are referred to as the basic building blocks, and the transconductor and multipliers are the circuits that take advantage of the building blocks, thus, the main effort is put when building the cells, and the cells are put together to build the transconductor and multiplier circuits. This also has an impact on the design time.

Fully integrated continuous time circuits can be realized in MOS technology by using MOS transistors operating in the triode region. MOS transistors used in filter applications for implementing linear resistors, suffer from nonidealities causing signal distortion such as body effect, mobility variation, device mismatch, etc. Extensive research has been conducted on the fully balanced integrator with MOS resistors, and a balanced two-MOSFET configuration was first introduced to cancel out even-order nonlinearities [26]. It was later demonstrated, using a strong inversion MOS model, that a four-MOSFET structure also fully suppresses the body effect related odd-order terms [27, 28]. However, recent works question the widely accepted superiority of the four-MOSFET structure [29]. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications [30, 31]. Therefore, it is of extreme importance to statistically examine the circuit. The four-MOSFET structure is reviewed in Chapter 3.

Digital-to-analog (D/A) converters interface the digital output of signal processors with the analog world, therefore, it is an essential function in data processing systems. The linearity of the D/A converter strongly depends on the accuracy of the reference multiplication or division employed to generate the output levels. The three electrical quantities, voltage, current and charge can be multiplied or subdivided using resistor ladders, current-steering circuits, and switched capacitor circuits, respectively. In this work the current division technique is used to divide the reference current in order to provide binary weighting, for a 10-bit example. The 10-bit current division network and its operation principle is given in Chapter 3.

Chapter 4 consists the main focus of this thesis. The statistical design and analysis of the circuits given in Chapter 3 will be discussed in detail, while providing experimental results for the four-MOSFET structure and the 10-bit current division network.

The CMOS square-law composite cells require highly matched currents flowing through the CMOS pair. Any mismatch in these currents will cause variations in the performance of the overall circuits which use the cells as a main building block, hence, the statistical examination of the relative drain current mismatch is important. It will be shown that statistical design is a crucial step in designing robust transconductor and multiplier circuits, since they depend on device matching to achieve a linearized characteristic. Response surfaces provided allow the circuit designer to be able to optimize the transistor sizes of the circuits before fabrication. Previously reported transconductor and multiplier works ignored the statistical approach in their design, hence, they can exhibit a wide variation in the offset and nonlinearity when manufactured in large numbers.

For exact cancellation of nonlinearities in the four-MOSFET structure, perfect matching is required, whereas random variations may not always allow for exact matching of the transistors. The previously done works have not considered random variations, hence it is important to quantitatively determine the effect of mismatches on nonlinearity cancellation. The experimental results will also be given in Chapter 4.

The achievable resolution of the D/A converter is an important design consideration. The D/A converter presented in Chapter 3 uses a 10-bit current division network in order to provide binary weighting. The current division network is based on the assumption of matched transistors, whereas, random variations may cause mismatch between transistors and a slight mismatch may cause an error which will limit the achievable resolution. Therefore, it is important to consider statistical simulations in the design of the D/A converter and to determine the error in terms of LSB units. The statistical design of the D/A converter based on the current division network is examined in detail in Chapter 4. Experimental results are provided.

Chapter 5 summarizes the work as well as discussing the results provided in Chapter 4. A conclusion together with future studies is given after this discussion.