

CHAPTER 3

LOW VOLTAGE LOW POWER ANALOG VLSI CIRCUITS

The need for the robust design of low voltage low power CMOS analog VLSI circuits is tremendously growing. There are three main driving forces that are pushing this growth:

- 1- Technology-driven forces
- 2- Design-driven forces
- 3- Market-driven forces

Technology-driven forces come from the reduction of the minimum feature size to scale down the chip area. Scaling down the transistor size can then integrate more circuit components in a single chip area and lower the cost. Also, smaller geometry usually lowers the parasitic capacitances, which means higher operating speed and lower power consumption. A decrease in MOS transistor size means reduced gate oxide thickness as well as reduced channel length. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced.

With the reduction of the device minimum feature size, millions of transistors can be fabricated on the same chip. This will result in a tremendous power consumption and cause excessive heating, which leads to the design-driven forces. Usually most of the chip area is occupied by the digital circuits and the average power consumption for digital circuits is proportional to the square of the power supply voltage. Thus, decrease

of the supply voltage reduces the power consumption in a significant amount. In analog circuits, however, reducing the supply voltage does not always mean lower power dissipation, hence, new design techniques for low power analog circuits are necessary to be developed.

The market-driven forces are noteworthy; e.g., current trends indicate that wireless mobile information technology within the next couple of decades will simply encompass the way of working, purchasing, playing, seeking service, purchasing products, by providing complete freedom of location to the individual. The individual demand for internet services, wireless cable television distribution, and information technology implies the development of broadband wireless mobile communications systems against current technology limits, such as the supply voltage and power dissipation.

All the above factors contribute to the necessity of low voltage and low power circuit solutions. Many applications which require reduced supply voltage and low power consumption are based on analog/digital, mixed-signal VLSI systems. The current trends of higher level of integration is leading to complete mixed-signal systems on a chip. One of the most important issues in mixed-signal design is the yield loss due to the analog portion of the chip. In most cases, the analog part will be much smaller than the digital portion, however, the analog part very much affects the overall yield of the chip. Therefore, it is important to make robust designs, to make sure that the yield loss due to analog components are minimized, such that it has little effect on the yield of the mixed-signal chip.

The main contribution of this thesis is the robust design methodology; using statistical models and techniques, to make a robust design of analog circuits. The statistical design of the analog circuits is demonstrated in Chapter 4, while this chapter describes the eight analog circuits that are statistically examined in the thesis. The circuits are selected among those which are subject to attention recently. The transconductor and multiplier circuits, however, are new designs for the thesis. The strategy behind these new designs are emphasized in the next page. All circuits are not the only examples of their types, and not the only circuits used for their purpose, but they certainly are one of the most popular, and recently used in several areas.

The first two circuits are analog CMOS cells which were previously designed for low voltage and low power applications. Both of the cells have a square-law characteristic. The description of these cells are given in detail.

The next four analog circuits, two transconductors and two multipliers, are newly designed for this thesis, and all four use the first two cells as a main building block, hence, understanding the basic principles of the low voltage and low power cells will lead to a better understanding of the transconductor and multiplier circuits.

One discussion is made for analog circuits being programmable as in the digital area. The long range goals are to make analog circuits programmable, and to realize applications involving analog computation. The goal is to come up with an analog design methodology similar to the one used for digital circuits, and take advantage of the basic building blocks. The low voltage and low power cells of this thesis are referred to as the basic building blocks, and the transconductor and multipliers are the circuits that take advantage of the building blocks, thus, the main effort is put when building the cells, and the cells are put together to build the transconductor and multiplier circuits.

Fully integrated continuous time circuits can be realized in MOS technology by using MOS transistors operating in the triode region. MOS transistors used in filter applications for implementing linear resistors, suffer from nonidealities causing signal distortion such as body effect, mobility variation, device mismatch, etc. It was demonstrated using a strong inversion MOS model, that a four-MOSFET structure fully suppresses the body effect related even- and odd-order terms. However, recent works question the widely accepted superiority of this structure. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications. Therefore, it is of extreme importance to statistically examine the circuit.

Digital-to-analog (D/A) converters interface the digital output of signal processors with the analog world, therefore, it is an essential function in data processing systems. The linearity of the D/A converter strongly depends on the accuracy of the reference multiplication or division employed to generate the output levels. The three electrical quantities, voltage, current and charge can be multiplied or subdivided using resistor

ladders, current-steering circuits, and switched capacitor circuits, respectively. In this work the current division technique is used to divide the reference current in order to provide binary weighting, for a 10-bit example.

All the above circuits were simulated using the MOSIS 2 μ m Level-2 n-well process parameters. The model parameters are listed in Appendix C. The power supply voltage for all circuits is 3V. All simulations were done using APLAC. The four-MOSFET structure and 10-bit current division network was fabricated through the MOSIS 2 μ m n-well process, experimental results will be given for these circuits.

3.1. LOW VOLTAGE AND LOW POWER CMOS SQUARE-LAW COMPOSITE CELLS

3.1.1. Low Voltage CMOS Square-Law Composite Cell

The low voltage square-law CMOS cell is described in this section. However, before going into the details of the cell, the reasons and the necessity of designing the low voltage and low power cells will be discussed.

The reasons of designing these cells go back to the single MOS transistor (Figure 3.1(a)). The single MOS transistor exhibits the square-law characteristic on the gate-source voltage. However, the low input impedance at the source of the transistor limits the applicability of the single transistor. The conventional composite transistor [37], given in Figure 3.1(b) was proposed in the late 1980s as a solution for this problem.

The circuit has one NMOS and one PMOS transistor placed in series. V_g is the equivalent gate voltage and V_s is the equivalent source voltage, and the high input impedance terminals control the current flow through the transistors. However, the conventional composite transistor has a high equivalent threshold voltage, given by

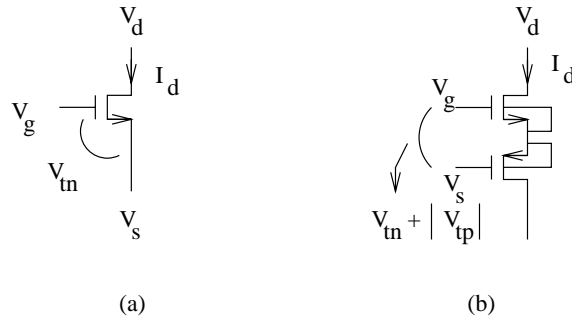


Figure 3.1: a) Single MOS transistor, b) Conventional composite transistor

$V_{Teq} = V_{Tn} + |V_{Tp}|$, where V_{Tn} and V_{Tp} are the threshold voltages of the NMOS and PMOS transistors, respectively, thus, making the threshold voltage almost twice as a single MOS transistor. This fact makes the circuit unsuitable for low voltage applications.

The low voltage square-law CMOS cell [38] was designed to overcome this drawback of the conventional composite transistor using the same idea. The currents flowing through both the NMOS and PMOS transistors are the same in the conventional composite transistor, which is given by $I_{dn} = I_{dp} = I_d$ in Figure 3.2(a). The sources of the transistors are connected to each other, and the condition $V_g - V_s > V_{Tn} + |V_{Tp}|$ should be satisfied, to keep the transistors in the on-state, which makes the range of the signal very small.

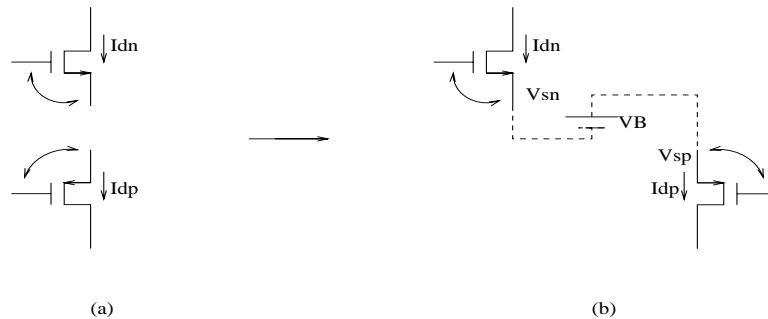


Figure 3.2: The basic idea of a) The conventional composite transistor, b) The low voltage square-law CMOS cell

The goal is to use the same idea but to reduce the equivalent threshold voltage, hence make the design suitable for low voltage applications. This could be done by adding a bias voltage, V_B , between the sources of the two transistors, instead of connecting them to each other. This will reduce the equivalent threshold voltage and the condition to keep the transistors on will be $V_g - V_s > V_{Tn} + |V_{Tp}| - V_B$, where the right-hand side value is less than the previous. This idea is illustrated in Figure 3.2(b).

The simplest way to accomplish this idea is to use a level shifter (Figure 3.3).

Δ , in Figure 3.3, is the shifted voltage value by the level shifter, which is basically the voltage difference between the voltages V_1 and V_2 .

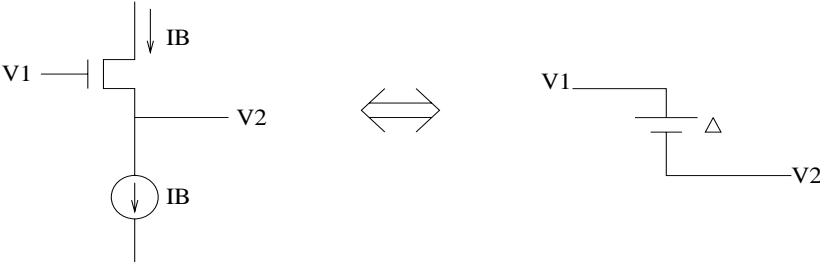


Figure 3.3: The idea of using a level shifter to reduce the equivalent threshold voltage

The implementation of the above described idea to build a low voltage cell [38] is illustrated in Figure 3.4.

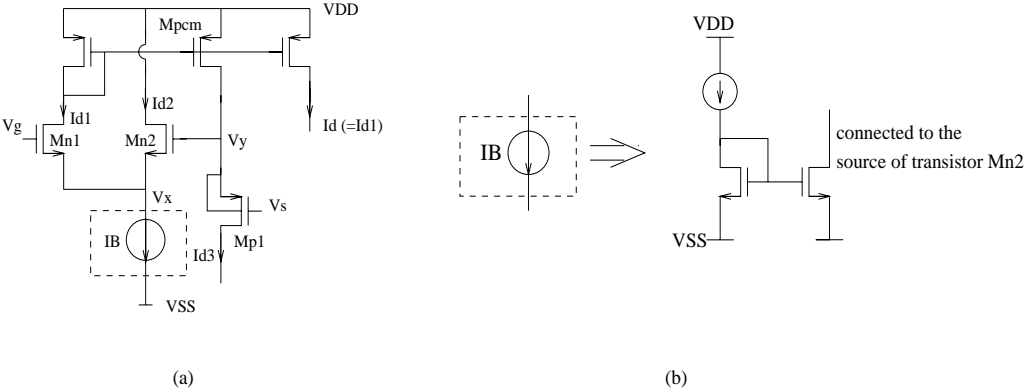


Figure 3.4: a) Low voltage CMOS square-law composite cell, b) Representation of the current source

Transistors M_{n1} and M_{p1} are the NMOS and PMOS transistors of the conventional composite transistor. The currents flowing through these transistors should be the same, and this is done by using a current mirror in the circuit. M_{pcm} is the group of PMOS transistors forming the current mirror to ensure that the currents flowing through transistors M_{n1} and M_{p1} are equal, by taking the current through M_{n1} and mirroring it to M_{p1} . M_{n2} and I_B form a level shifter to decrease the value of the effective threshold voltage. The drain currents I_{d1} through I_{d3} shown in Figure 3.2 are expressed as

$$I_{d1} = \frac{K_{n1}}{2}(V_g - V_x - V_{Tn})^2 \quad (3.1)$$

$$I_{d2} = \frac{K_{n2}}{2}(V_y - V_x - V_{Tn})^2 \quad (3.2)$$

$$I_{d3} = \frac{K_{p1}}{2}(V_y - V_s - |V_{Tp}|)^2 \quad (3.3)$$

Using the fact that $I_{d1} = I_{d3} = I_d$ and $I_{d1} + I_{d2} = I_B$, equations (3.1) through (3.3) can be rewritten in the form of

$$V_g - V_x = \sqrt{\frac{2I_d}{K_{n1}}} + V_{Tn} \quad (3.4)$$

$$V_y - V_x = \sqrt{\frac{2(I_B - I_d)}{K_{n2}}} + V_{Tn} \quad (3.5)$$

$$V_y - V_s = \sqrt{\frac{2I_d}{K_{p1}}} + |V_{Tp}| \quad (3.6)$$

The drain current equation for the low voltage CMOS square-law composite cell can be then written as

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \quad (3.7)$$

where K_{eq} and V_{Teq} is the equivalent transconductance parameter and the equivalent threshold voltage, respectively, expressed as

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}} \right)^{-2} \quad (3.8)$$

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2(I_B - I_d)}{K_{n2}}} \quad (3.9)$$

It is clear that the threshold voltage is much less than the threshold voltage of the conventional composite transistor, hence the goal of designing a cell which has a square-law characteristic, and which is suitable for low voltage applications is reached. However, the threshold voltage equation given by equation (3.9) quickly reflects the drawback of this cell; that is, the threshold voltage is a function of the drain current, I_d . Hence, the threshold voltage is varying with the input voltage causing distortion.

One way to avoid this is to keep the bias current, I_B , much larger than I_d , so that I_d in equation (3.9) will be canceled, thus, the threshold voltage equation can be simplified as

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2I_B}{K_{n2}}} \quad (3.10)$$

which is now a constant value and still much less than the equivalent threshold voltage of the conventional composite transistor. However, the condition $I_B \gg I_d$ means that it is not possible to arbitrarily reduce the bias current, I_B , to obtain an improved power consumption, which brings a trade-off to the cell, between low voltage operation and low power dissipation. This trade-off is also the main drawback of this cell and will be reflected to the circuits that are using the cell as a main building block. It is possible to overcome this trade-off between low voltage operation and low power dissipation, though, and the next section will describe another cell, again using the same original

idea with the conventional composite transistor, with a method to keep the threshold voltage constant.

Finally, the DC transfer curve of the low voltage square-law CMOS cell is given in Figure 3.5.

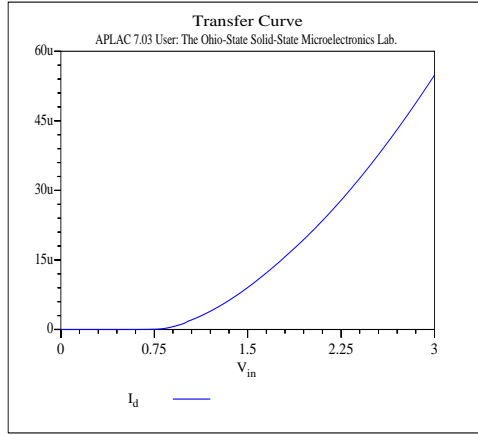


Figure 3.5: DC transfer curve of the low voltage square-law CMOS cell

The W/L values of the transistors in the circuit are given in Table 3.1.

Table 3.1: W/L values of the transistors of the low voltage square-law CMOS cell. The bias current is $I_B=120\mu A$

Transistors	M_{n1}	M_{n2}	M_{pcm}	M_{p1}	M_{ncs}
W/L	5/2	100/2	150/3	15/2	38/3

M_{ncs} represents the transistors that were used for I_B , as shown in Figure 3.4(b).

Simulations were done for the source voltage of $V_s=0.5V$, and the gate-source voltage of $V_{gs}=2V$. The bias current was $120\mu A$, and the supply voltage was $3V$. The simulations were done using APLAC, and the netlist is given in Appendix D.

3.1.2. Low Voltage Low Power CMOS Square-Law Composite Cell

As mentioned in the previous section, the drawback of the low voltage cell is that it simply has to satisfy the condition, $I_B \gg I_d$, for a constant threshold voltage, which brings a trade-off between low voltage operation and low power dissipation to the circuit. The problem is that the current flowing through transistor M_{n1} , in Figure 3.4, is $(I_B - I_d)$, thus varying, which means that the V_{GS} of transistor M_{n1} is varying with current. The current flowing through transistor M_{n1} should be constant, even for a varying I_d .

One way to achieve this is to put a constant current source, I_B , to the drain of transistor M_{n1} , as shown in Figure 3.6.

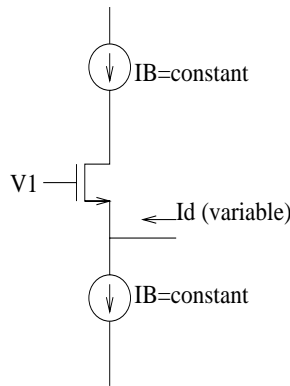


Figure 3.6: Constant current source at the drain of the transistor, for keeping the drain current of the transistor constant

In Figure 3.6, the current going to the drain of the transistor is a constant I_B , and the current going out from the source is a constant I_B as well, whereas the variable drain current, I_d , is also going into the source of the transistor, which brings a contradiction. A simple way to avoid this is to make the I_B (connected to the source of the transistor) variable, e.g., if I_d increases, I_B will automatically increase to accommodate this change of current. Two NMOS transistors will be connected to the circuit, which will take place of I_B (the one connected to the source of the transistor), as shown in Figure 3.7.

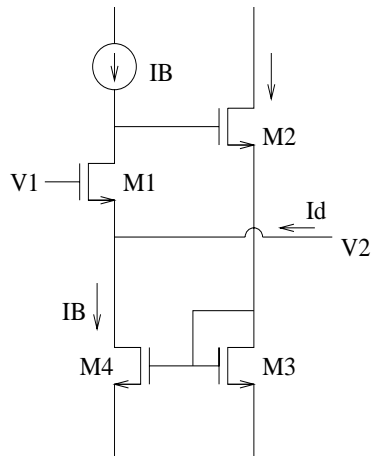


Figure 3.7: The feedback loop that will keep the threshold voltage constant without having to satisfy any condition for the bias current

I_B is coming from the current mirror transistors M_3 and M_4 . It is mirrored by the current mirror and this current should be dependent on the drain current, I_d . This is accomplished by the feedback transistor M_2 ; if I_d increases the current flowing through transistor M_2 should increase, and if I_d decreases the current flowing through transistor M_2 should also decrease. The next paragraph explains how this is done with the help of the illustration in Figure 3.8.

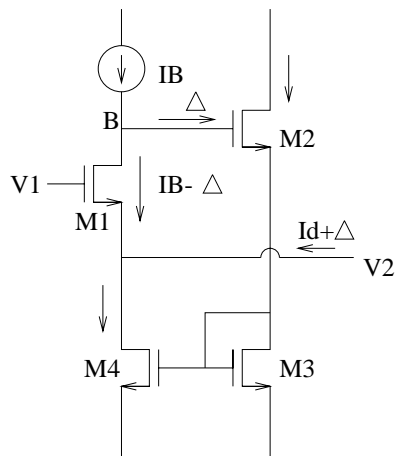


Figure 3.8: The description of the feedback loop

The drain currents I_{d1} through I_{d3} shown in Figure 3.9 are expressed as

$$I_{d1} = \frac{K_{n1}}{2}(V_g - V_x - V_{Tn})^2 \quad (3.12)$$

$$I_{d2} = \frac{K_{n2}}{2}(V_y - V_x - V_{Tn})^2 \quad (3.13)$$

$$I_{d3} = \frac{K_{p1}}{2}(V_y - V_s - |V_{Tp}|)^2 \quad (3.14)$$

Since $I_{d1} = I_{d3} = I_d$ and $I_{d2} = I_B$, the above equations can be rewritten as

$$V_g - V_x = \sqrt{\frac{2I_d}{K_{n1}}} + V_{Tn} \quad (3.15)$$

$$V_y - V_x = \sqrt{\frac{2I_B}{K_{n2}}} + V_{Tn} \quad (3.16)$$

$$V_y - V_s = \sqrt{\frac{2I_d}{K_{p1}}} + |V_{Tp}| \quad (3.17)$$

Substituting equations (3.15) and (3.17) in equation (3.16) will give

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \quad (3.18)$$

where K_{eq} and V_{Teq} are the equivalent transconductance parameter and the equivalent threshold voltage, respectively, expressed as

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}} \right)^{-2} \quad (3.19)$$

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2I_B}{K_{n2}}} \quad (3.20)$$

Equation (3.20) shows that the circuit no longer has to satisfy $I_B \gg I_d$, as I_d can be increased regardless of I_B . The trade-off between low voltage operation and low power dissipation for the previous cell has been overcome in this circuit.

The DC transfer curve of the low voltage low power square-law CMOS cell is given in Figure 3.10, for a bias current of $I_B=120\mu A$, $V_s=0.5V$ and $V_{gs}=2V$, and for a supply voltage of 3V.

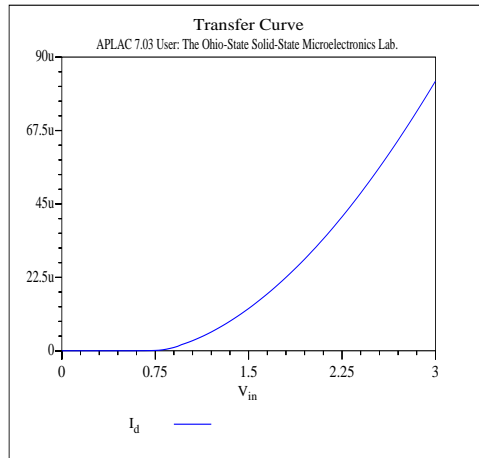


Figure 3.10: The DC transfer curve of the low voltage low power square-law CMOS cell

The W/L values of the transistors in the low voltage low power square-law CMOS cell are given in Table 3.2.

Table 3.2: W/L values of the transistors of the low voltage low power square-law CMOS cell. The bias current is $I_B=120\mu A$

Transistors	M_{n1}	M_{n2}	M_{pcm}	M_{n3}	M_{p1}	M_{n4}, M_{n5}	M_{pcs}
W/L	5/2	100/2	150/3	500/2	15/2	38/3	150/3

M_{pcs} represents the transistors that were used for I_B , as shown in Figure 3.9(b). The simulations were done using APLAC, and the netlist is given in Appendix E.

3.1.3. Summary of the Square-Law CMOS Cells

Many applications which require reduced supply voltage and low power consumption are based on analog/digital mixed-signal VLSI circuits. A certain class of these circuits are basically composed of several cells which have a square-law characteristic. A single MOSFET fulfills this characteristic, however, the low input impedance at the source of the transistor limits the applicability of the single transistor solution. The conventional composite transistor was proposed as a solution for this problem. However, the conventional composite transistor is not suitable for low voltage applications because of its high equivalent threshold voltage. Recently, several new low voltage and low power CMOS square-law composite cells with two high impedance input terminals were proposed to achieve accurate signal processing with low power dissipation. The design and operation principles of two of these cells were described in detail, in the previous sections. Understanding the basic principles of the low voltage and low power cells will lead to a better understanding of circuits which use these cells as a main building block.

Two new transconductors and multipliers were built using the low voltage and low power cells. These circuits will be discussed next, after a brief introduction on linear transconductors.

3.2. LINEAR TRANSCONDUCTORS

MOS transconductors are useful building blocks for the design of analog and mixed-signal systems. Such applications usually require very linear transconductance elements with a good high frequency capability. An elegant way to achieve a linear transconductor, starting with transistors in strong inversion and having a square-law behavior, is to use the difference of squares principle [40]. This principle states that given the variables A and B, the difference of the squares $(A+B)^2$ and $(A-B)^2$ is linear in A or B, that is

$$[(A+B)^2 - (A-B)^2]^2 = 4AB \quad (3.21)$$

This principle can be used to arrive a linear relationship between the difference in the gate-source voltages of two transistors and the difference in their output currents. The realizations given in [37, 41, 42, 43] are based on using MOS transistors operating in the saturation region.

The new transconductors that will be introduced in the next two sections are using the low voltage and low power CMOS square-law cells of Section 3.1 as their main building block. Note that, when using these cells as a building block, the advantages and disadvantages of the cells will be also reflected to the circuits which are using them.

3.2.1. Transconductor Using the Low Voltage CMOS Square-Law Composite Cell

The transconductor using the low voltage CMOS square-law composite cell is illustrated in Figure 3.11 [44].

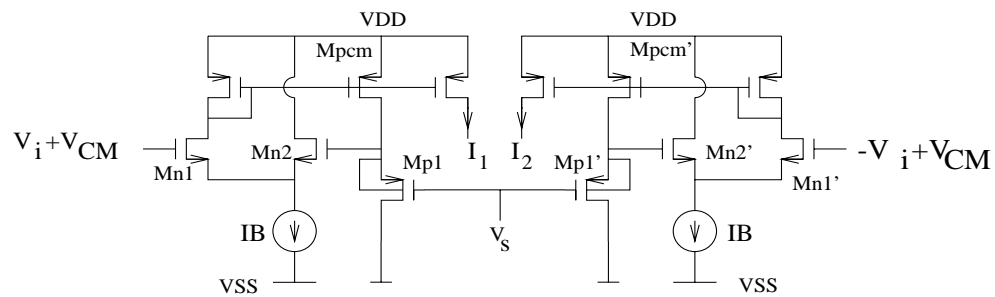


Figure 3.11: The transconductor using the low voltage CMOS square-law composite cell

The low voltage square-law CMOS composite cells are connected in such a way to build a transconductor. The circuit operates in the saturation region with a fully balanced input signal. It is preferable that analog circuits operate in the fully balanced mode, mainly because fully balanced circuits ensure high power supply rejection, improve linearity and increase dynamic range. The input voltages and the control voltage are applied to the NMOS and PMOS pair, respectively. The output differential current equation is derived by using the difference of squares principle:

$$I_1 - I_2 = K_{eq}(V_{gs1} - V_{Teq})^2 - K_{eq}(V_{gs1} - V_{Teq})^2$$

$$I_1 - I_2 = K_{eq}[(V_i + V_{CM} - V_s - V_{Teq})^2 - K_{eq}(-V_i + V_{CM} - V_s - V_{Teq})^2]$$

$$I_1 - I_2 = 4K_{eq}(V_{CM} - V_s - V_{Teq})V_i \quad (3.22)$$

Hence, the transconductance is given by

$$G_m = 4K_{eq}(V_{CM} - V_s - V_{Teq}) \quad (3.23)$$

where K_{eq} and V_{Teq} is the equivalent transconductance parameter and the equivalent threshold voltage, respectively.

Tunability is a very important parameter for transconductors. The transconductance is affected by the threshold voltage and transconductance parameter, which change with temperature (30% typical value). Thus, it is important for the transconductor to be tunable to compensate process and temperature variations. Note that, having the control voltage, V_s , in equation (3.23) allows the transconductance of the circuit to be electronically tuned.

The low voltage cell had a trade-off between low voltage operation and low power dissipation, hence, the transconductor will have the same trade-off as well, since it is using the cell as a main building block.

The DC transfer curve of the transconductor using the low voltage square-law CMOS cell is given in Figure 3.12.

The input voltage is applied to the NMOS transistors and is $V_i = \pm 0.3$ V and the common mode voltage is $V_{CM} = 2$ V. The control voltage is $V_s = 0.6$ V and the bias current is $I_B = 120 \mu$ A. The transfer curve is obtained by sweeping V_s from 0.2 V to 0.6 V, with a 0.1 V increment. I_o is the output current defined as $I_o = I_1 - I_2$.

The netlist of the circuit is given in Appendix F.

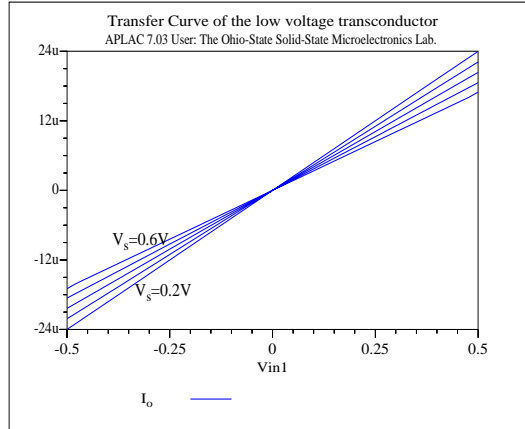


Figure 3.12: The DC transfer curve of the transconductor using the low voltage CMOS square-law composite cell

It is noteworthy that, the input voltage, V_i , can be applied either to the NMOS or the PMOS transistor, in which case the control voltage, V_s , will be applied to the other. In both cases the transconductance will be the same, however, because of the fact that NMOS transistors are faster than PMOS transistors, and also because the output path for the transconductor with inputs on the PMOS pair is longer than the other, the circuit will be faster when inputs are on the gates of the NMOS pair.

3.2.2. Transconductor Using the Low Voltage Low Power CMOS Square-Law Composite Cell

Figure 3.13 shows the transconductor [45] using the low voltage low power square-law CMOS composite cell as a building block. The trade-off between low voltage operation and low power dissipation is avoided with the use of the low voltage low power cell.

The main points of the low voltage transconductor that were emphasized in the previous section, are valid for this transconductor as well. The circuit operates in the saturation region with a fully balanced input signal. The inputs are applied to the NMOS pair and the control voltage, and V_s , is applied to the PMOS pair in the circuit. The transconductance of the circuit is derived by taking the difference of the output currents of each cell:

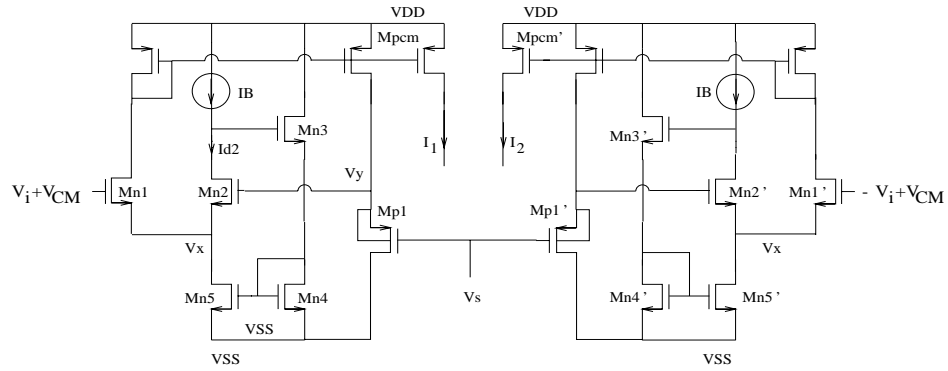


Figure 3.13: The transconductor using the low voltage low power CMOS square-law composite cell

$$G_m = 4K_{eq}(V_{CM} - V_s - V_{Teq}) \quad (3.24)$$

which is similar to equation (3.23).

Figure 3.14 shows the DC transfer curve of the transconductor using the low voltage low power square-law CMOS cell, where I_o is the output current and is defined by $I_o = I_1 - I_2$. The same biasing conditions that were applied to the previous transconductor is used to bias the low voltage low power transconductor: The input voltage is $V_i = \pm 0.3$ V, and is applied to the NMOS transistors of the transconductor. The common mode voltage is $V_{CM} = 2$ V. The control voltage is $V_s = 0.6$ V and the bias current is $I_B = 120 \mu$ A. The transfer curve is obtained by sweeping the control voltage, V_s , from 0.2 V to 0.6 V, with a 0.1 V increment.

The netlist of the circuit is given in Appendix G.

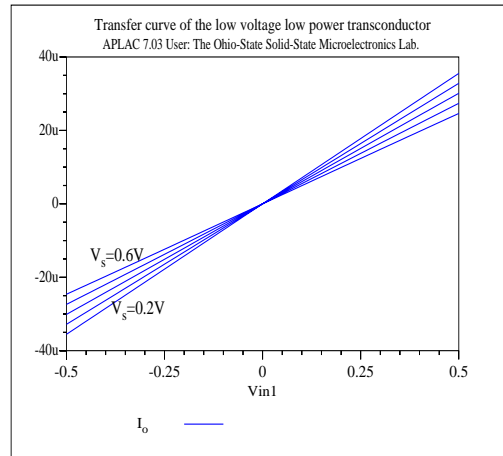


Figure 3.14: The DC transfer curve of the transconductor using the low voltage low power CMOS square-law composite cell

3.3. ANALOG MULTIPLIERS

Analog multipliers are essential building blocks found in a wide range of applications including communications, analog signal processing and neural networks. Multiplier designs have received much of the attention, and may be implemented in a variety of ways including the technique using the square-law characteristic of MOS transistors in the saturation region [46-49]. Many applications require linear multipliers and matching is very important to obtain highly linear multipliers no matter what the implementation is.

Two new multipliers which use the low voltage and low power square-law cells are introduced in this section.

3.3.1. Multiplier Using the Low Voltage CMOS Square-Law Composite Cell

The multiplier using the low voltage CMOS square-law composite cell is illustrated in Figure 3.15 [48].

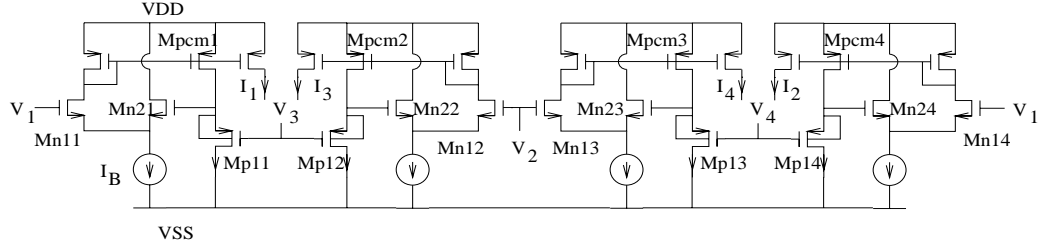


Figure 3.15: Multiplier using the low voltage CMOS square-law composite cell

The circuit can be viewed as the parallel connection of two transconductors introduced in Section 3.2.1, or the combination of four low voltage CMOS square-law cells. The circuit operates in the saturation region with a fully balanced input signal. The output current of the multiplier can be written in terms of the input currents as

$$I_0 = (I_1 + I_4) - (I_2 + I_3) \quad (3.25)$$

where I_1 , I_2 , I_3 and I_4 are the input currents.

The multiplier consists of four low voltage CMOS square-law composite cells, and these cells have a square-law characteristic, hence, the input currents can be written as square-law equations;

$$I_1 = \frac{K_{eq}}{2}(V_1 - V_3 - V_{Teq})^2 \quad (3.26)$$

$$I_2 = \frac{K_{eq}}{2}(V_1 - V_4 - V_{Teq})^2 \quad (3.27)$$

$$I_3 = \frac{K_{eq}}{2}(V_2 - V_3 - V_{Teq})^2 \quad (3.28)$$

$$I_4 = \frac{K_{eq}}{2}(V_2 - V_4 - V_{Teq})^2 \quad (3.29)$$

Substituting equation (3.26) through (3.29) into equation (3.25) will give the output current equation in terms of the input voltages:

$$I_o = K_{eq}(V_1 - V_2)(V_4 - V_3) \quad (3.30)$$

where K_{eq} is the equivalent transconductance parameter and V_1 , V_2 , V_3 and V_4 are the input voltages of the circuit. The input voltage range of the analog multiplier is usually restricted to a fraction of the power supply voltage, hence, it is convenient to express the input voltages in terms of a differential voltage superimposed as a common mode voltage:

$$V_1 = V_{CM1} + \frac{\Delta v_{12}}{2} \quad (3.31)$$

$$V_3 = V_{CM2} + \frac{\Delta v_{34}}{2} \quad (3.32)$$

$$V_2 = V_{CM1} - \frac{\Delta v_{12}}{2} \quad (3.33)$$

$$V_4 = V_{CM2} - \frac{\Delta v_{34}}{2} \quad (3.34)$$

where V_{CM1} and V_{CM2} are the input common mode voltages, and input differential voltages denoted by Δv_{12} and Δv_{34} are defined as

$$\Delta v_{12} = V_1 - V_2 \quad (3.35)$$

$$\Delta v_{12} = V_3 - V_4 \quad (3.36)$$

Figure 3.16 shows the transfer curve of the multiplier using the low voltage CMOS square-law composite cell.

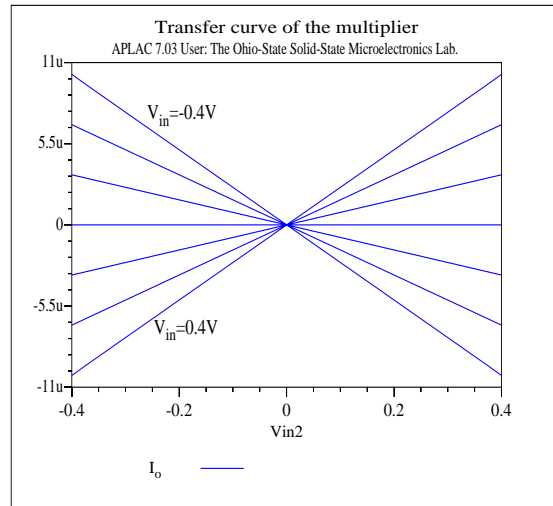


Figure 3.16: The DC transfer curve of the multiplier using the low voltage CMOS square-law composite cell

Simulations were done with APLAC, for a 3V supply voltage and a bias current of $I_B=120\mu\text{A}$. The input voltages are $\mp 0.3\text{V}$ for V_1 and V_2 , and V_3 and V_4 . The common mode voltages for the inputs V_1 and V_2 , and V_3 and V_4 are 2.4V and 0.6V, respectively. The netlist of the circuit is given in Appendix H.

Note that the trade-off between low voltage operation and low power dissipation exists for the multiplier, since the main block of the circuit has this trade-off.

3.3.2. Multiplier Using the Low Voltage Low Power CMOS Square-Law Composite Cell

Figure 3.17 shows the multiplier using the low voltage low power CMOS square-law composite cell [49].

Unlike the previously introduced multiplier, the circuit does not have a trade-off between low voltage operation and low power dissipation, since the circuit is a combination of four low voltage low power cells, and this cell overcomes this trade-off.

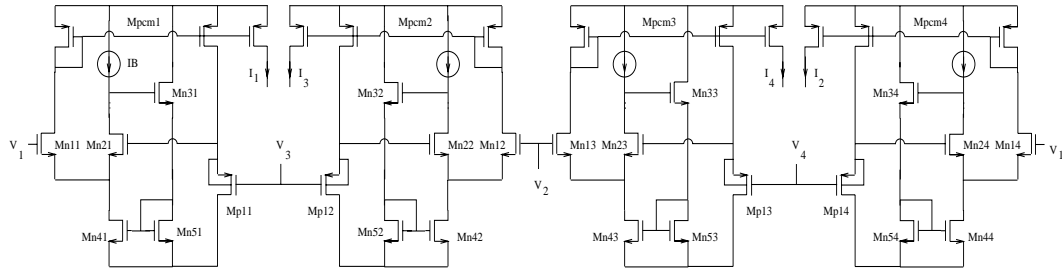


Figure 3.17: Multiplier using the low voltage low power CMOS square-law composite cell

It is possible proceed as in the previous multiplier circuit, to arrive to the output current of the circuit, in terms of the input voltages:

$$I_o = K_{eq}(V_1 - V_2)(V_4 - V_3) \quad (3.37)$$

The transfer curve of the circuit was obtained for the same biasing conditions used for low voltage multiplier. Simulations were made with APLAC, using a 3V supply voltage. The transfer curve of the multiplier using the low voltage low power CMOS square-law composite cell is given in Figure 3.18.

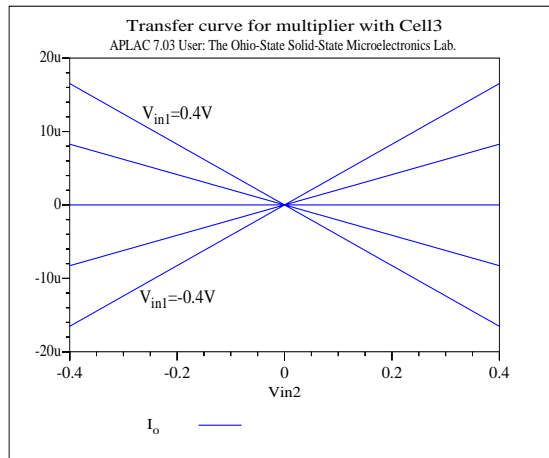


Figure 3.18: The DC transfer curve of the multiplier using the low voltage low power CMOS square-law composite cell

The netlist of the circuit is given in Appendix I.

3.4. THE FOUR-MOSFET STRUCTURE AND A DISCUSSION FOR NONLINEARITY CANCELLATION

Fully integrated continuous time circuits can be realized in MOS technology by using MOS transistors operating in the triode region. MOS transistors used in filter applications for implementing linear resistors suffer from nonidealities causing signal distortion such as body effect, mobility variation, device mismatch, etc.

Extensive research has been conducted on the fully balanced integrator with MOS resistors. It was demonstrated, using a strong inversion MOS model, that a four-MOSFET structure fully suppresses the even and odd-order nonlinearity terms [26, 27]. However, recent works question the widely accepted superiority of the four-MOSFET structure [28]. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications [29, 30].

For exact cancellation of nonlinearities, exact transistor matching is needed, whereas, random variations may not always allow for exact matching of transistors. Most of the previously done four-MOSFET structure works have not considered random variations, hence, it is important to quantitatively determine the effect of mismatches on nonlinearity cancellation.

The four-MOSFET structure is reviewed in this section.

3.4.1. Four-MOSFET Structure

The four-MOSFET structure is illustrated in Figure 3.19.

All transistors in the circuit are operating in the triode region. The output voltages V_{o1} and V_{o2} , must be equal, i.e. $V_{o1} = V_{o2} = V$, to achieve nonlinearity cancellation. The operation of the circuit depends on the perfect matching of transistors; any mismatch will cause distortion.

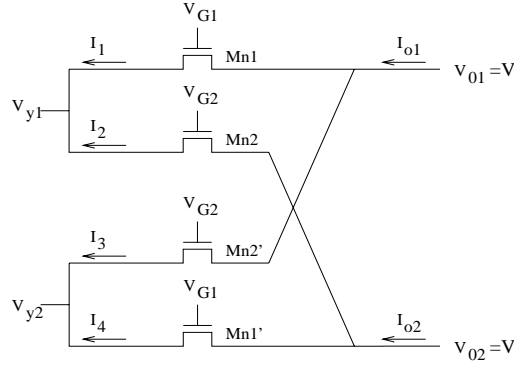


Figure 3.19: The four-MOSFET structure

The output current is given by

$$I_o = (I_1 + I_3) - (I_2 + I_4) \quad (3.38)$$

where I_1 , I_2 , I_3 and I_4 are triode region currents given by

$$I_1 = K_1 \left(V_{G1} - V_{y1} - V_T - \frac{1}{2}(V - V_{y1}) \right) (V - V_{y1}) \quad (3.39)$$

$$I_2 = K_2 \left(V_{G2} - V_{y1} - V_T - \frac{1}{2}(V - V_{y1}) \right) (V - V_{y1}) \quad (3.40)$$

$$I_3 = K_3 \left(V_{G2} - V_{y2} - V_T - \frac{1}{2}(V - V_{y2}) \right) (V - V_{y2}) \quad (3.41)$$

$$I_4 = K_4 \left(V_{G1} - V_{y2} - V_T - \frac{1}{2}(V - V_{y2}) \right) (V - V_{y2}) \quad (3.42)$$

Assuming perfect matching of the transistors will result in $K_1 = K_2 = K_3 = K_4 = K$. As equations (3.39) through (3.42) are placed in equation (3.38), the output current of the four-MOSFET structure is found as

$$I_o = K(V_{G1} - V_{G2})(V_{y2} - V_{y1}) \quad (3.43)$$

The transfer curve of the Four-MOSFET structure for the aspect ratios of $W/L=4/4$ and $W/L=20/4$ are shown in Figure 3.20.

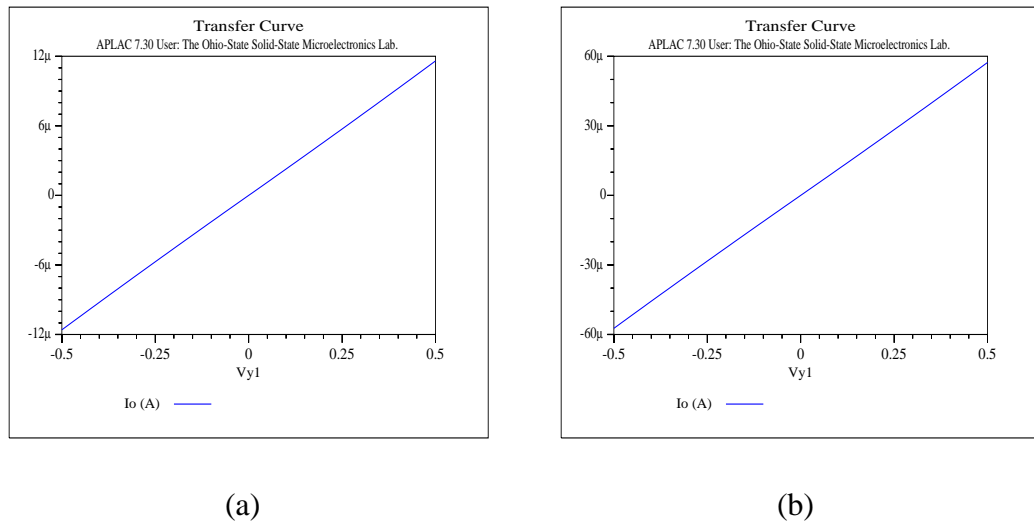


Figure 3.20: The DC transfer curve of the four-MOSFET structure (APLAC simulation results), for a) $W/L=4/4$, b) $W/L=20/4$

Simulations were done using APLAC, for a 3V supply voltage. The circuit is biased as $V_{o1}=V_{o2}=0.8V$, $V_{G1}=2.2V$, $V_{G2}=2.75V$, $V_{y1}=1.1V$ and $V_{y2}=0.5V$. The netlist is given in Appendix J.

The four-MOSFET structure was fabricated through the MOSIS $2\mu m$ process, using MOS transistor Level-2 model parameters, for the aspect ratios of $W/L=4/4$ and $W/L=20/4$. The experimentally found transfer curve for both aspect ratios are shown in Figure 3.21.

The experimental results are obtained with the help of the HP4145B parameter analyzer. Measurements were made on 4 tiny MOSIS chips, each one having 15 samples of the four-MOSFET structure, 7 samples for the aspect ratio of $W/L=4/4$ and 8 samples for aspect ratio of $W/L=20/4$. The results are discussed in Chapter 4.

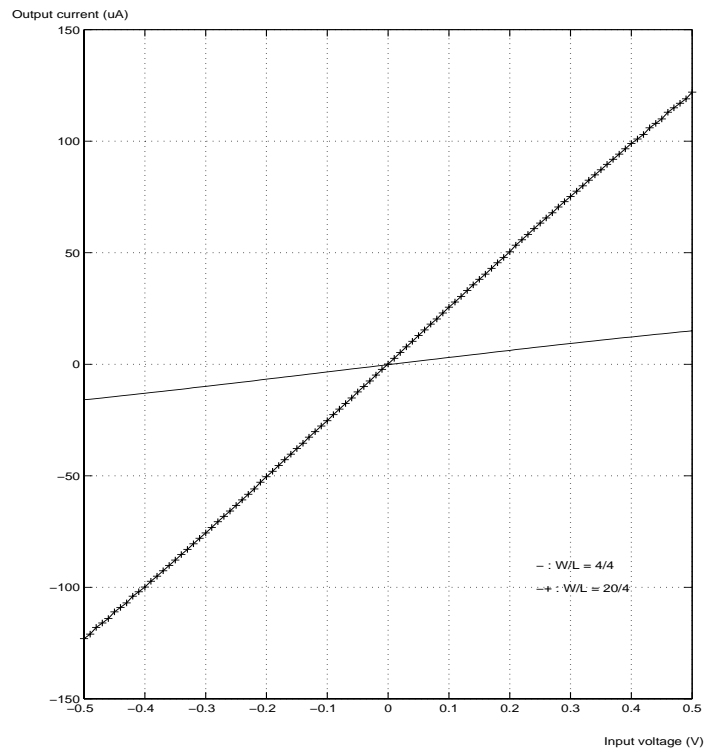


Figure 3.21: The DC transfer curve of the four-MOSFET structure (experimental results) for aspect ratios $W/L=4/4$ and $W/L=20/4$

3.5. D/A CONVERTER BASED ON THE CURRENT DIVISION TECHNIQUE

Data conversion provides the link between the analog world and digital systems, and is performed by means of sampling circuits, A/D converters, and D/A converters. With the increasing use of digital computing and signal processing applications such as medical imaging, instrumentation, consumer electronics, and communications, the field of data conversion systems rapidly expanded over the past years [50, 51]. D/A converters interface the digital output of signal processors with the analog world, therefore, it is an essential function in data processing systems.

The main concentration in this thesis is on the linearity of the D/A converters. The linearity strongly depends on the accuracy of the reference multiplication or division employed to generate output levels. The three electrical quantities, voltage, current and charge can be multiplied or subdivided using resistor ladders, current-steering circuits, and switched capacitor circuits, respectively. In this work, a current division network will be used to divide the reference current in order to provide binary weighting, for a 10-bit example.

A technique for dividing currents accurately and linearly is useful for various kinds of analog signal processing applications. A common technique is to use resistors or capacitors for the linear and accurate division of current while using MOS transistors as switches or amplifying elements [52, 53].

The MOS transistor can be used for signal division, thus, eliminating the need for resistors or capacitors. Although an MOS transistor exhibits a nonlinear relationship between current and voltage, the current division function is inherently linear [54].

This section describes the 10-bit current division network and its operation principle.

3.5.1. The 10-bit Current Division Network

The 10-bit current division network is illustrated in Figure 3.22.

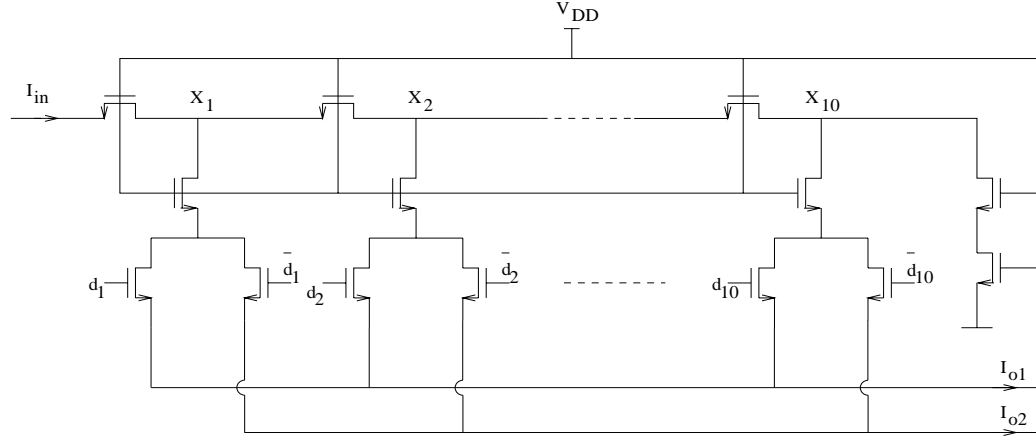


Figure 3.22: The 10-bit current division network

The input current, I_{in} , flowing towards node X_1 is divided equally into two as $I_{in}/2$ at this node. This current is flowing through one of the NMOS transistors, according to d_1 being logic 0 or logic 1. The current entering node X_2 has the value of $I_{in}/2$ and is equally divided as $I_{in}/4$. Again, this current is flowing through one of the NMOS transistors, so forth. The current value of $I_{in}/2^9$ will enter node X_{10} and this current will be divided having the value of $I_{in}/2^{10}$. This will lead to a general expression for the current as

$$I_i = I_{in} \times (2^{-i} d_i) \quad (3.44)$$

where I_i is the current value after being divided at node X_i , I_{in} is the input current, and d_i is the gate voltage of the NMOS transistors, either logic 0 or logic 1. The I_i values contribute to the output currents I_{o1} and I_{o2} [55] which are given by

$$I_{o1} = I_{in} \sum_{i=1}^{10} 2^{-i} d_i \quad (3.45)$$

$$I_{o2} = I_{in} \sum_{i=1}^{10} 2^{-i} \bar{d}_i \quad (3.46)$$

Figure 3.23 shows the transfer curve of the 10-bit current division network for the aspect ratio of $W/L=44/4$, and for two different digital word settings;

$$d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$$

$$d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$$

Simulations were done for an input current of $I_{in}=100\mu A$. The netlist is given in Appendix K

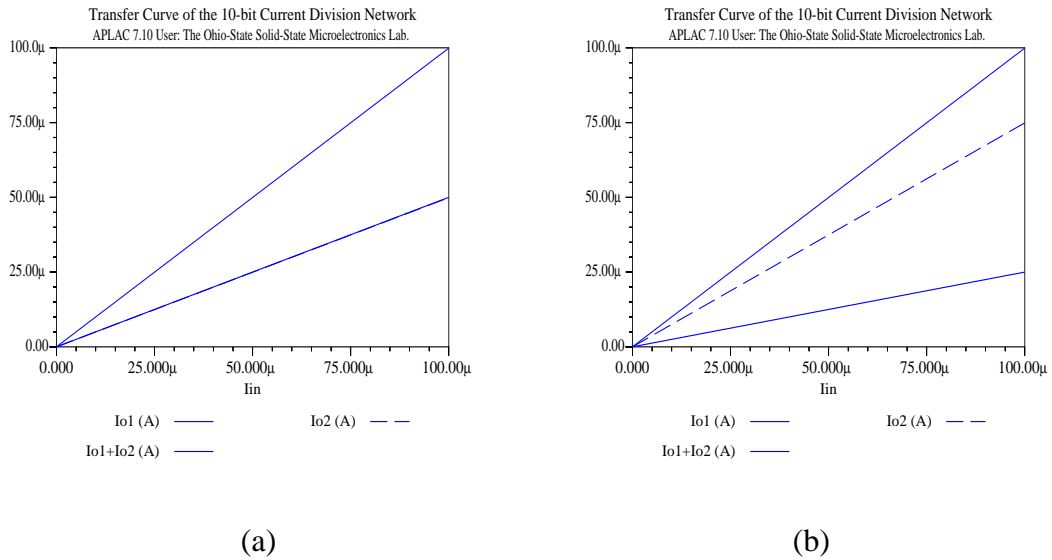
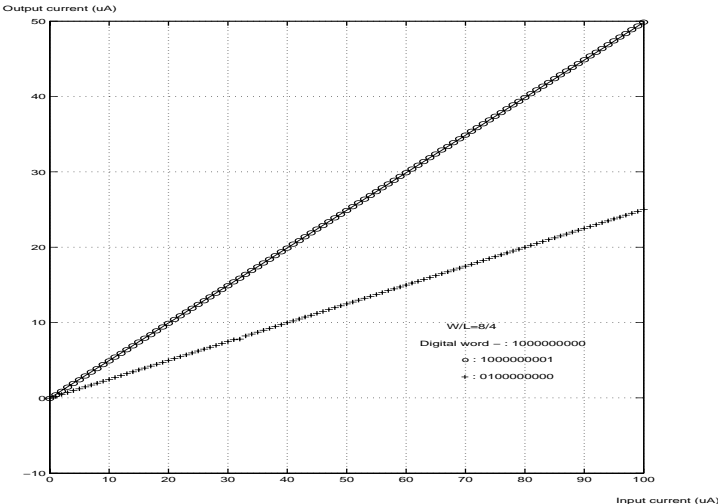
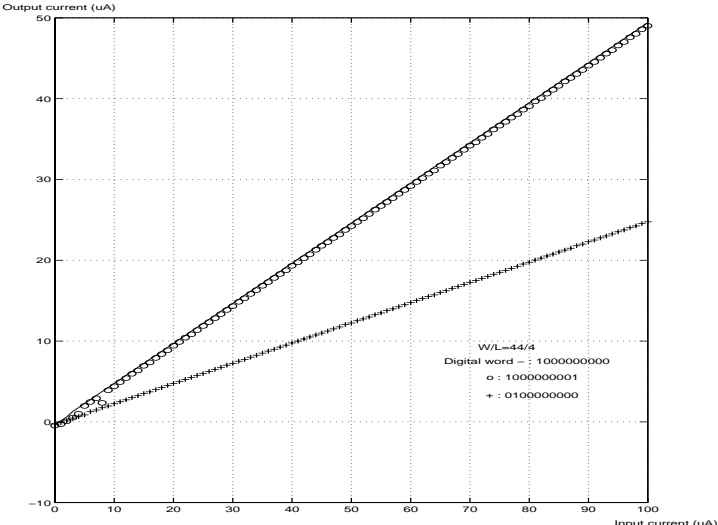


Figure 3.23: Transfer curve of the 10-bit current division network (APLAC simulation results), for the aspect ratio of $W/L=44/4$, and for digital word settings; a) $d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$ and b) $d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$

The 10-bit current division network was fabricated through the MOSIS 2 μ m process, using MOS transistor Level-2 model parameters, for the aspect ratios of $W/L=8/4$ and $W/L=44/4$. The transfer curve for both aspect ratios and the two different digital word settings given above are shown in Figure 3.24.



(a)



(b)

Figure 3.24: Transfer curve for the 10-bit current division network (experimental results) for two digital word settings; $d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$; $d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$; a) $W/L=8/4$, b) $W/L=44/4$

The experimental results for the 10-bit current division network were obtained using the HP4145B parameter analyzer. Measurements were made on 4 tiny MOSIS chips, each one having 11 samples of the 10-bit current division network, 6 samples for the aspect ratio of $W/L=44/4$, and 5 samples for the aspect ratio of $W/L=8/4$. The results are discussed in Chapter 4.