ECE 6194.08 (Proposed): Group Studies: Design and Process Integration for Wide Band Gap Power Devices

Course Description

Design and processing of wide band gap power devices (including SiC, GaN and ultra wide band gap semiconductors) and reliability considerations. 2D device simulations, layout considerations for power chip design, optimization of performance and reliability/qualification for various voltage ranges from 600 V to 15 kV.

Transcript Abbreviation: GrStd Pwr Chip Des
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Graduate
Student Ranks: Masters, Doctoral
Course Offerings: Autumn
Flex Scheduled Course: Never
Course Frequency: Every Year
Course Length: 14 Week
Credits: 3.0
Repeatable: No
Time Distribution: 3.0 hr Lec
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: Grad standing in engineering or physics.
Exclusions:
Cross-Listings:

Course Rationale: Update and expand curriculum to include design of modern power devices.

The course is required for this unit's degrees, majors, and/or minors: No
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code:
Subsidy Level:

Course Goals

Provide an introduction to basic operation of WBG power devices
Students master design principles and 2D simulations of power devices
Students become competent with layout of Power device chips
Students are exposed to the processing details of power devices
Students become familiar with reliability and qualification of power devices

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Review of semiconductor basics	4.0							
Operation and characteristics of the SiC Schottky Barrier Diode, SiC DMOSFET and GaN HEMT	4.0							
2D simulations of 1700 VSiC Schottky Barrier Diode, DMOSFETS and 600 V GaN HEMT and design considerations for edge termination, dv/dt, short circuit time, avalanche ruggedness, design for HTRB, optimization of on-resistance etc.	9.0							
Process Integration: Overall process sequence for SiC Schottky Diode, SiC MOSFET and GaN HEMT and unit processes	9.0							
Layout of the 1700 V SiC Schottky Barrier Diode, DMOSFET and 600 V GaN HEMT	9.0							
Misc. Topics: Thermal and yield considerations, qualification and reliability, cost of manufacturing, availability of substrates and epilayers, Worldwide manufacturing of SiC and GaN devices and supply chain	5.0							

Representative Assignments

Individual projects to design SiC DMOSFETS (Integrated Body Diode) and GaN HEMT for various voltages. Each student will be assigned a unique device and a unique voltage and current rating

Grades

Aspect	Percent
Individual projects submitted in several steps along the semester	100%

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
*	a	An ability to apply knowledge of mathematics, science, and engineering.
*	b	An ability to design and conduct experiments, as well as to analyze and interpret data.
***	c	An ability to design a system, component, or process to meet desired needs.
	d	An ability to function on multi-disciplinary teams.
**	e	An ability to identify, formulate, and solve engineering problems.
	f	An understanding of professional and ethical responsibility.
	g	An ability to communicate effectively.
	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
	i	A recognition of the need for, and an ability to engage in life-long learning.
	j	A knowledge of contemporary issues.
**	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Additional Notes or Comments

`Prepared by: Anant Agarwal`

Prepared by: Anant Agarwal