ECE 3561: Advanced Digital Design

Course Description

Design and analysis of sequential circuits; digital circuit design using building blocks, programmable logic devices; design of basic computer components such as arithmetic logic units.

Prior Course Number: 561, 667
Transcript Abbreviation: Adv Digital Dsgn
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Undergrad
Student Ranks: Junior, Senior
Course Offerings: Autumn, Spring
Flex Scheduled Course: Never
Course Frequency: Every Year
Course Length: 14 Week
Credits: 3.0
Repeatable: No
Time Distribution: 3.0 hr Lec
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: Prereq: 2000, 2060, 2061, 2010, 2000.02, 290, 294 (Autumn 2010) or 206 and 261. Prereq or concur: 3020 (323), and enrollment in ECE, EngPhys, or CSE majors; or prereq or concur 2010 and permission of department.
Exclusions: Not open to students with credit for 561.
Cross-Listings:

Course Rationale: Existing course.

The course is required for this unit's degrees, majors, and/or minors: Yes
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code: 14.0902
Subsidy Level: Baccalaureate Course

Programs

Abbreviation	Description
CpE	Computer Engineering
EE	Electrical Engineering

Course Goals

Learn digital design principles and practice and learn to design using building blocks such as counters, shift registers, and adders and programmable logic devices such as FPGAs and CPLD
Learn methods to design clocked sequential circuits using state diagrams and tables, state reduction and state assignment methods
Learn to perform timing analysis at each step of the design

VHDL is introduced
Design and simulate digital circuits using a state-of-the-art CAD package. Both schematic and VHDL-based design is supported

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Clocked synchronous state-machine analysis and timing	8.0							
Clocked synchronous state-machine design	13.0							
Design with counters, shift registers, multiplexers, comparators, decoders, and adders	8.0							
Design with asynchronous inputs and for glitch-free outputs	1.0							
VHDL for combinational logic and state machine design	4.0							
Logic implementation with PLDs, FPGAs, and ROMs	6.0							

Representative Assignments

Textbook problems
Computer simulations

Grades

Aspect	Percent
Quizzes	15%
Computer Projects & Homework	30%
Midterm Exams	25%
Final Exam	30%

Representative Textbooks and Other Course Materials

Title	Author
Fundamentals of Logic Design	Roth and Kinney

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
***	a	An ability to apply knowledge of mathematics, science, and engineering.
*	b	An ability to design and conduct experiments, as well as to analyze and interpret data.
***	c	An ability to design a system, component, or process to meet desired needs.
**	d	An ability to function on multi-disciplinary teams.
***	e	An ability to identify, formulate, and solve engineering problems.
*	f	An understanding of professional and ethical responsibility.
*	g	An ability to communicate effectively.
	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
**	i	A recognition of the need for, and an ability to engage in life-long learning.
	j	A knowledge of contemporary issues.

Course Contribution		College Outcome
***	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Additional Notes or Comments

deleted "ECE" from exclusion of 567- BLA 2/22/12

Add "; or prereq or concurrent 2010 and permission of department." to prereq 10/20/13

Make consistent with university version 2/13/14

Add a star to ABET outcome "b' per ABET review 4/21/14 BLA

Add 2060, 2061 to prereqs 9/8/2015 BLA

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