ECE 5462 (Proposed): HDL Design and Verification

Course Description

The detailed design and verification of major components of a computer architecture using a standard hardware description language (HDL).

Prior Course Number: 762, 764
Transcript Abbreviation: HDL Dsgn and Verif
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Undergrad, Graduate
Student Ranks: Junior, Senior, Masters, Doctoral
Course Offerings: Autumn
Flex Scheduled Course: Never
Course Frequency: Every Year
Course Length: 14 Week
Credits: 3.0
Repeatable: No
Time Distribution: 3.0 hr Lec
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: Prereq: 5362, or 561 and 662, or CSE 675.01 or equiv, or Grad standing in Engineering.
Exclusions: Not open to students with credit for 762 or 764.
Cross-Listings:

Course Rationale: Existing course.

The course is required for this unit's degrees, majors, and/or minors: No
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code: 14.0902
Subsidy Level: Doctoral Course

Programs

Abbreviation	Description
CpE	Computer Engineering
EE	Electrical Engineering

Course Goals

Introduce design of major components of computer architecture
Introduce basic concepts of hardware description languages (HDL)
Learn to use VHDL to specify, design, and model digital hardware components
Learn functional verification and implement a verification plan on HDL designs. Verification of a complex component and a system of several components is done

Learn to use HDL computer aided design tools

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Advanced logic design techniques, computer architecture	6.0							
Basic of a Hardware Description Language	6.0							
Modeling of basic digital hardware	5.0							
Modeling of complex digital hardware	10.0							
Verification approaches, testing of designs, verification tools, simulators	3.0							
The verification plan, levels of verification and verification strategies	2.0							
Architecting testbenches, stimulus and response, self-checking testbenches	4.0							
PSL and assertion based verification	4.0							

Representative Assignments

A series of project steps on the design of a processor data path is followed to intoduce the student to various styles of HDL modeling.
HDL modeling of a state machine.
HDL modeling of a floating point execution unit.
Verification of the HDL model of a floating point execution unit.
Verification modeling of an execution subunit of a processor architecture.

Grades

Aspect	Percent
Individual modeling projects	30%
Verification projects - group assignment	20%
Midterm Exam	25%
Final Exam	25%

Representative Textbooks and Other Course Materials

Title	Author
VHDL: Analysis and Modeling of Digital Systems, 3rd ed. ISBN: 978-0071475457	Zain Navabi

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
***	a	An ability to apply knowledge of mathematics, science, and engineering.
***	b	An ability to design and conduct experiments, as well as to analyze and interpret data.
***	c	An ability to design a system, component, or process to meet desired needs.
**	d	An ability to function on multi-disciplinary teams.
**	e	An ability to identify, formulate, and solve engineering problems.
*	f	An understanding of professional and ethical responsibility.

Course Contribution		College Outcome
*	g	An ability to communicate effectively.
	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
*	i	A recognition of the need for, and an ability to engage in life-long learning.
*	j	A knowledge of contemporary issues.
***	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Additional Notes or Comments

corrected prereqs to delete 4362, old course number.
Corrected typos in text, 4/3/12.
Updated text to 3rd edition, 6/6/13. CED.

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