ECE 5194.08 (Proposed): Group Studies: Advanced Hardware Architecture Design Techniques

Course Description

This course introduces highly-practical methodologies and techniques that can be broadly used to improve the efficiency and achieve speed-area-power tradeoffs in the design of hardware implementation architectures for various algorithms. Efficient implementation architectures of commonly used arithmetic and digital signal processing functional blocks will also be discussed.

Transcript Abbreviation: Adv Hardware Arch
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Undergrad, Graduate
Student Ranks: Senior, Masters, Doctoral
Course Offerings: Spring
Flex Scheduled Course: Never
Course Frequency: Every Year
Course Length: 14 Week
Credits: 3.0
Repeatable: No
Time Distribution: 3.0 hr Lec
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: 2050, and prereq or concurrent: 3561 or 3050; or permission of instructor, or Grad standing in engineering.
Exclusions:
Cross-Listings:

Course Rationale: This course covers highly practical design techniques that can be easily applied to improve

the hardware implementation efficiency of various systems

The course is required for this unit's degrees, majors, and/or minors: No
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code: 14.1001
Subsidy Level: Doctoral Course

Programs

Abbreviation	Description
CpE	Computer Engineering
EE	Electrical Engineering

Course Goals

Students are exposed to advanced definitions and concepts relevant to the design of digital logic architectures.
Students become familiar with hardware architecture design methodologies for trading off speed, silicon area, and power consumption.
Students become competent in the design of efficient architectures for commonly used arithmetic and digital signal processing functional blocks.

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Characteristics and representations of signal processing programs	1.0							
Iteration bound	3.0							
Pipelining and parallel processing	3.5							
Retiming	3.5							
Unfolding	3.5							
Folding	3.5							
Fast Convolution	3.0							
Algorithmic strength reduction in filters and transformations	3.0							
Pipelined and parallel recursive filters	3.0							
Bit-level arithmetic architecture	3.0							
Redundant Arithmetic	2.0							
Numerical strength reduction	1.0							
Various implementation topics	6.0							

Representative Assignments

Homework
Midterms
Project

Grades

Aspect	Percent
Midterm 1	30%
Midterm 2	30%
Final project	40%

Representative Textbooks and Other Course Materials

Title	Author
VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley & Sons, 1999. ISBN 0-471-24186-5	K. K. Parhi

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
***	a	An ability to apply knowledge of mathematics, science, and engineering.
	b	An ability to design and conduct experiments, as well as to analyze and interpret data.

Course Contribution		College Outcome
***	c	An ability to design a system, component, or process to meet desired needs.
	d	An ability to function on multi-disciplinary teams.
*	e	An ability to identify, formulate, and solve engineering problems.
	f	An understanding of professional and ethical responsibility.
	g	An ability to communicate effectively.
	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
*	i	A recognition of the need for, and an ability to engage in life-long learning.
	j	A knowledge of contemporary issues.
**	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

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